A New Sigma-Delta Modulator Architecture for Testing Using Digital Stimulus

Chee-Kian Ong, Student Member, IEEE, Kwang-Ting (Tim) Cheng, Fellow, IEEE,
Li-C. Wang, Member, IEEE

***Abstract* – Sigma-delta modulators are commonly used in high-resolution ADCs. Testing this type of modulator requires a high-resolution test stimulus, which is difficult to generate. A new architecture for the modulator is proposed so that its performance can be determined using only digital test stimulus. This architecture does not need analog test stimuli, which is prone to distortion/noise while setting up the high-resolution modulator for testing. Simulation results show that this technique is capable of accurately determining the performance of a second-order sigma-delta modulator ADC.**

***Keywords*: Sigma-delta, ADC testing, digital stimulus, Built-In Self-Test, design-for-testability**

I. INTRODUCTION

Oversampled sigma-delta modulation has gained much popularity in analog-to-digital conversion application since it was first proposed four decades ago. The sigma-delta modulator Analog-to-Digital converter (ADC) is based on the principle of trading time resolution for amplitude resolution, i.e. it converts an analog signal into a high-speed (tens of Nyquist rate) but low-resolution (typically single-bit) digital signal. The digital signal is digitally filtered to extract the information of the analog signal at a high resolution. With the continuing scaling of the transistor size, digital filters are getting cheaper to implement. With the modulator's robustness to the imperfection of analog implementation, the sigma-delta modulator is suitable for integrated circuit implementation especially for System-on-chip (SoC) designs. Other applications based on the sigma-delta modulation technique include digital telephony, digital signal processing, instrumentation, digital audio, and Built-In Self-Test (BIST) for mixed-signal circuits [1, 2, 3, 4, 5, 6].

Testing ADC is mostly limited to conventional static and dynamic testing. Generally in static testing, DC levels with increment of ¼ LSB (Least Significant Bit) are applied to the input of the ADC in order to achieve ½ LSB accuracy in differential and integral non-linearity measurement. The outputs of the ADC are analyzed to determine the differential and integral non-linearity of the ADC [7]. In this case, the signal generator needs to generate a stimulus with resolution at least four times higher than that of the ADC under test. In the case of dynamic testing, the test stimulus with known characteristics is applied to the ADC under test [7]. The output of the ADC is captured and analyzed using, but not limited to, sinewave fitting or Fast Fourier Transform (FFT). In both cases, the test stimuli must have a resolution better than that of the ADC under test, and they can be very expensive to generate.

Reports [1, 2, 3, 4, 5, 6, 8] have shown that band-limited test stimulus can be easily generated on-chip using the sigma-delta modulation technique. All mentioned methods require additional analog filters and voltage references to complete the stimulus generation and are intended for general analog/mixed-signal test application. Noises and process variation from these analog components would have direct effect on the stimulus, and these reports have yet to mention how to measure or ensure the quality of the test stimulus. Thus, further test, which has yet to be mentioned, is required for these built-in circuitries to ensure the quality of the generated stimuli. Recently, a technique [9] is reported using a pseudo-random sequence to test the second-order modulator by characterizing the latter's parameters. However, this method relies on characterizing limited modulator parameters, which may not accurately determine the modulator performance.

A new architecture for the sigma-delta modulator, hereafter known as the design-for test (DfT) sigma-delta architecture, is proposed in [10] to enable the use of digital stimulus to determine the modulator performance. Along with the DfT architecture, a new testing technique and the type digital stimulus required to digitally test the architecture is also presented. Since the DfT modulator requires only digital bit stream as test stimulus, generating analog stimulus to test the modulator is not required. This feature is important since generating analog signal can be very challenging especially for signal with high-resolution requirement. This DfT modulator can be easily enhanced into a BIST solution in a System-on-Chip (SoC), which usually has on-chip processor that can be used to generate the digital test stimulus and analyze the modulator performance [11]. This paper is organized as follows. Section 2 giving a brief description on the background of a second-order sigma-delta modulator and its non-ideal model. Section 3 describes the new test technique and the proposed DfT modulator architecture that enables normal digital stimulus to achieve high quality Signal-to-Noise Ratio (SNR) measurement for the sigma-delta modulator. Section 4 presents the simulation results to demonstrate the technique's capability measuring a second-order sigma-delta modulator's SNR. The concluding section discusses the issues of the proposed technique and DfT architecture.

II. BACKGROUND

Sigma-delta modulators are commonly known as noise-shaping modulators due to their quantization noise association with a differential function that shapes the noise frequency spectrum. The differential function suppresses in-band frequency components of the quantization noise. The order of a modulator is determined by the differential function order. A higher-order modulator has a higher differential function order, which yields more suppression on the in-band quantization noise. The differential function also makes sigma-delta modulation ADCs gain more resolution than those conventional ADCs when sampling rates are increased.

For an L-order sigma-delta modulator, the in-band noise falls $3(2L + 1)$ decibels for every doubling of the sampling rate, providing $(L+1/2)$ extra bits of resolution [12] (for ADC without noise shaping, $L = 0$). Hence, the resolution of the modulator can be improved by increasing either the sampling rate or the order of the modulator. However, a modulator with an order greater than two becomes unstable and difficult to implement

[12]. The modulator's resolution can also be improved by using multi-bit quantizer. However, multi-bit quantizer will require a multi-bit DAC in the modulator feedback loop. This type of modulator requires precise matching between the quantizer decision levels and the output level of the feedback DAC. This matching limits the resolution of the modulator and induces unwanted non-linearity into the modulator characteristic. Unlike the multi-bit modulator, a single-bit modulator has a quantizer with only one decision level, and a 1-bit DAC in its feedback loop. The implementation of the 1-bit DAC in the loop is easy and highly linear, since there is only one decision level in the quantizer. Today, most applications use a second-order single-bit sigma-delta modulator, even for applications with 24-bit resolution [13,14].

A. The Second-Order Sigma-delta Modulator

In 1985, Candy introduced the second-order sigma-delta modulator [15]. Our study is based on the model introduced by Lainey et al. [16], which is shown in Figure 1. This modulator is easier to implement, as both of its integrators introduce a unit-sample delay into the signal path [17]. Shown in Figure 1, the modulator consists of two integrators, one quantizer and a Digital-to-Analog converter (DAC) in the feedback loop. Each integrator consists of an adder, a delay block, and a unit feedback loop.

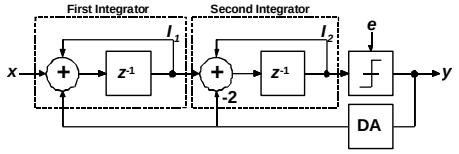

Figure 1 The block diagram of a second-order ΣΔ modulator

The block diagram is presented in z transform domain and z^{-1} denotes a sample delay. Prior to the output y is a two-level quantizer, which is a comparator that compares the second integrator output, I_2, with its threshold. It is common in analysis to model the quantizer as an adder of its input, I_2, and a random quantization noise, e. Hence, the output of the modulator can be represented by the following equations:

$$y_i = x_{i-2} + e_i - 2e_{i-1} + e_{i-2} \quad (1)$$

$$y = xz^{-2} + e\left(1 - z^{-1}\right)^2 \quad (2)$$

Eq. 2 is the z transform of the difference Eq. 1. As shown in Eq. 2, the quantizer error, e, is associated with a second-order differential function $(1\text{-}z^{-1})^2$.

B. The Non-Ideal Model

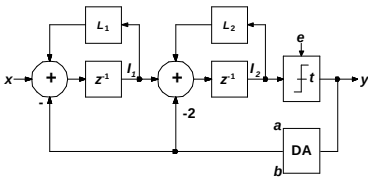

Figure 2 Non-ideal second-order modulator block diagram

When the second-order modulator is implemented in silicon, its behavior deviates from the ideal model. Some additional parameters are required to model the non-ideal behavior. The non-ideal model used in our study is adapted from [18], as shown in Figure 2.

In Figure 2, L_1 and L_2 are the leakage factors associated with the practical leaky integrators. For an ideal integrator the leakage factor is one, and for a leaky integrator less than one. Parameter t is the threshold of the two-level quantizer (for an ideal quantizer, t=0). The upper and lower output levels of the DA are designated as a and b, respectively. For an ideal DA, a=1, b=-1. For differential modulators, $a = -b$, because the output voltages for the DA are interchanged when the DA input changes logic state. For example, the differential DA output for a logic `1' is represented by $V_{ref+} - V_{ref-}$, corresponding to $a$. Hence, the differential output for a logic `0' will be represented by $V_{ref-} - V_{ref+}$, corresponding to b. Any variation on the two reference voltages, V_{ref+} and V_{ref-}, will not change the fact that $a = -b$. Since most modulators are differential, we will assume this condition in our analysis. With this assumption, variations of a and b will only affect the output of the DA converter and directly reflect on the input range of the modulator.

III. THE PROPOSED DFT MODULATOR ARCHITECTURE

Generating test stimulus with resolution above 18-bit, even externally, is very challenging. Hence, testing converters with very high resolution has been limited to static test, as generating dynamic test stimulus, like sinewave, with resolution beyond 18-bit can be very costly. Static test method requires long test time, since each ADC output code has to appear a few times during the test to build a histogram, which is used to calculate the converter linearity. However, this method is unable to measure the converter noise component, which determines the ADC SNR.

This section covers the measurement technique, which uses digital stimulus to test the modulator, and the DfT modulator architecture, which enable its internal reference voltages to generate the required digital stimulus to enable high-quality performance measurement.

A. Digital Stimulus Measurement Technique

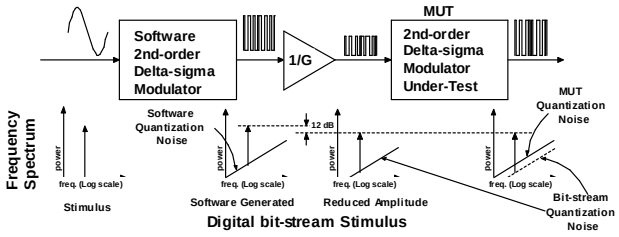

Figure 3 Digital Stimulus Measurement Technique (DSMT)

Figure 3 shows the overview of the digital stimulus measurement technique (DSMT). This technique uses a digital stimulus, which is encoded with an analog signal, to excite the MUT. Then the MUT SNR is calculated as the ratio of the analog signal power to the MUT noise power within the specification bandwidth. First, a sinewave stimulus is numerically modulated into a digital bit-stream using an ideal second-order sigma-delta modulator model. Then, the bit-stream amplitude is reduced before applying it to the second-order sigma-delta modulator under test. The purpose for the amplitude reduction is to maintain the stability of the modulator under test (MUT). Through simulation, it is found that the largest allowable amplitude of the bit-stream without causing

instability to the modulator is around ¼ of the modulator's input range, which is determined by the modulator's quantizer levels. To ensure that maximum possible analog signal strength is applied to the MUT, it is desirable to use the largest allowable amplitude during measurement. Therefore amplitude of the bit stream is reduced to ¼ of the modulator's input range.

The amplitude reduction of the bit-stream also reduces the floor level of the digital stimulus quantization noise, which is introduced into the digital bit-stream spectrum during the modulation process. Hence, using the DSMT, the quantization noise floor of the MUT dominates that of the digital stimulus at the MUT output . This allows us to determine the noise component of the MUT, and hence, determine the MUT SNR. However, the amplitude reduction of the bit-stream to ¼ reduces the sinewave signal power by 12 dB at the input and the output of the MUT. Hence, the digital stimulus measurement technique (DSMT) results in a calculation loss of 12 dB in the MUT SNR as compared to that of conventional testing where the analog stimulus is directly applied to the MUT. Hence, after calculating the SNR of the MUT using the proposed technique, a 12dB gain is added to derive the actual MUT SNR. Note that the MUT SNR is calculated using the FFT as it is used in the conventional dynamic testing.

The digital bit-streams can also be generated on-chip by implementing the digital portion of the sigma-delta modulated oscillators [2]. Additional DAC or analog filtering mentioned in [2] is not required since this test technique requires only the digital bit-stream.

B. The DfT Sigma-delta Modulator Architecture

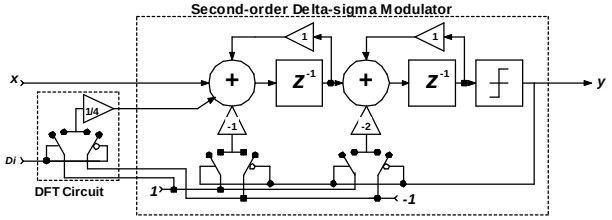

Figure 4 A DfT Second-order Sigma-delta Modulator

The sigma-delta modulator needs to be modified to facilitate and to enhance the accuracy of the proposed measurement technique. Figure 4 shows the block diagram of the DfT sigma-delta modulator architecture. The 1-bit DAC in the feedback loop of the sigma-delta modulator is normally implemented with switches controlled by the quantizer digital output. The digital-to-analog conversions are realized when the quantizer output selects either of the positive or negative reference voltages to the input of the adders. The only difference between this DfT modulator and the traditional one is the additional DfT circuit shown in Figure 4. The DfT circuitry enables the use of the modulator reference voltages to test modulator, and hence, avoids generating additional reference voltages. Through the digital input *Di*, the digital stimulus selects either of the two reference voltages to the gain block. Then the DfT gain block reduces the selected reference voltage by a factor of 4 before applying it to the first adder of the modulator. This is equivalent to generating a digital bit-stream with ¼ the level of reference voltages. Hence, the quality and precision of the actual digital stimulus applied to the modulator is equivalent to that of the reference voltage.

Note that to apply the digital stimulus through the input channel, additional reference voltages equivalent to ¼ of the MUT reference voltages would be required, as would additional tests to measure these additional reference voltages before applying them to the MUT. Such requirements would make the measurement technique less appealing. Since the proposed DfT technique enables the use of the MUT reference voltages to generate the test stimulus, both the accuracy of the proposed measurement technique and the modulator's performance are prone to the same noise effect and parameter variations. Simulation results presented in the next section show that the measurement technique can achieve measurement accuracy within 1 LSB of the MUT with noise and level deviations injected into the reference voltages. The range of noise level and level deviation is discussed in the next section. When the MUT is implemented using switch-capacitor filters, the gain stage in the DfT circuit can be implemented using the capacitor-matching principle, which reduces mismatch error to tenth of a thousand. A matching error of 3×10^{-4} is equivalent to a deviation of 0.0026 dB ($20\log[1 - 3\times10^{-4}]$) in the SNR calculation. This error is negligible considering the overall DSMT accuracy, which is discussed in the later section.

During testing, the MUT analog input *x* is disconnected from the MUT. This can be easily done, by including an analog switch at the input channel prior to the MUT. For modulators implemented using switched capacitor networks, we can disable the clocks that transfer the charges from the input capacitor to the first adder and integrator.

In this DfT modulator, however, the digital stimulus is applied directly to the first adder instead of the input channel. We assume that the channel to the input of the modulator is properly laid out and shielded using ground tracks, thus minimizing interference from neighboring tracks, if any. One thing left to test is the continuity of the input channel from the input pad of the die to the input of the MUT. The continuity of the input channel can be tested by applying two different reference voltages to the input pad and observing the number of logic one occurrences at the output of the MUT over a given period. If the input channel is not broken, the modulator will generate a larger logic-one count when the larger reference voltage is applied to the input pad. Hence, by applying two different reference voltages to the input pad, we look for different logic-one counts at the output of the MUT to determine the continuity of the input channel. The difference between the two reference voltages should be large enough to generate significant difference in the logic-one counts within a short period (typically tens of samples range). Although, this test does not require accurate reference voltages, we can apply the MUT's reference voltages to the input pad for this test. This test can be easily modified to test bridging fault between the input channel and the shielding-ground tracks. In this case, the resistance of the bridging fault would results in a different voltage at the MUT input, when one of the reference voltages is applied to the input pad. However, to determine the input voltage of the MUT with higher accuracy, longer observation time would be required. Hence, to accurately determine the bridging fault resistance a longer observation time is needed.

Note that the only required test stimulus in this measurement technique is a bit-stream of digital signal, which does not require precise levels. And the only additional analog circuit

required for the DfT modulator is the gain stage, which is implemented using the capacitor-matching principle to reduce the gain error resulting from process variation. When the modulator is implemented using a switch-capacitor network, the gain stage(s) to the adder input, the adder, and the integrator following the adder are normally implemented as a single entity. Switched-capacitor implementation reduces the gain matching errors among the gain stages at the input of the adder.

C. Digital Filtering

Digital filtering, also known as *Decimation*, is performed at the modulator output to enable robust selection on segment of the filtered signal to perform Fast Fourier Transformation (FFT) to calculate the modulator SNR. Performing FFT directly on different segments of the modulator output, which would yield different SNR, can be avoided with decimation. Decimation is a process for converting the bit-stream to the desired pulse code modulation (PCM) at a lower sampling rate through a digital smoothing and re-sampling process [12]. In this process, the bit-stream is digitally filtered and down-sampled. A factor M down-sampling is a process in which the signal sampling rate is reduced by M. This is equivalent to selecting one out of M samples from the signal. This section discusses the design of a simple comb filter that minimizes the coefficient word length, eliminates the need for a high-speed parallel multiplier, and reduces the memory storage requirement. The aliasing effect associated with sampling and down-sampling will also be discussed.

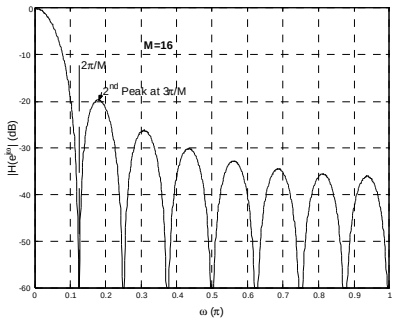

Figure 5 Frequency response of sinc3 filter with M=16

The Comb filters, also known as the *sinc* filters, are very attractive for implementation because they do not require the use of a digital multiplier. Although they are often used with another digital filter to achieve the desired PCM sampling rate, this application requires only the sinc filters. They are most efficiently implemented by cascading K stages of accumulators operating at the sampling rate of the modulator, followed by K stages of cascaded differentiators operating at the down-sampled rate [19]. The transfer function and frequency response for a sinc filter with K stages and a down-sample factor M has the general form of

$$H(z)=\left(\frac{1}{M}\frac{1-z^{-M}}{1-z^{-1}}\right)^K \tag{3}$$

$$\left|H(e^{jw})\right|=\left(\frac{1}{M}\frac{\sin(\omega M/2)}{\sin(\omega/2)}\right)^K \tag{4}$$

Figure 5 shows the frequency response of the $sinc^K$ filter with M = 16. Signal frequency components are shaped by the sinc filter frequency response when the signal passed through the filter. The desired frequency components within the signal bandwidth should be contained within the first peak of the sinc filter frequency response, and their attenuation should not be larger than 3 dB. This constrain the sinc filter parameters as follows

$$20\log\left[\left(\frac{1}{M}\frac{\sin(\omega M/2)}{\sin(\omega/2)}\right)\right] > -3dB \tag{5}$$

$$\text{where;} \quad \omega < 2\pi f_b / f_s$$

where f_b is the bandwidth of the desired signal. When a signal is down-sampled by a factor M, its frequency components, whose frequencies fall within $2\pi/M$, will be aliased by those whose frequencies are greater than $2\pi/M$. To retain the quality of the signal after down-sampling, the second peak of the filter frequency response has to be low enough to minimize the alias effect. Hence, the sinc filter design is constrained by its parameters satisfying

$$20\log\left[\left(\frac{1}{M}\frac{\sin(\omega M/2)}{\sin(\omega/2)}\right)\right] > -130dB \tag{6}$$

$$\text{where;} \quad \omega < 3\pi / M$$

for reconstructing a signal with 130 dB SNR. The largest peak of the filter frequency response for $\omega > 2\pi/M$ occurs at $\omega = 3\pi/M$. In general, a larger K will yield a larger attenuation and a larger M will yield more, and hence thinner, peaks in the filter frequency response.

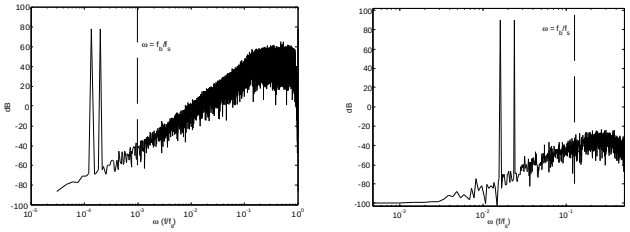

Figure 6 Frequency spectrum of a sigma-delta modulated bit-stream and its *sinc* filtered signal

The diagram on the left of Figure 6 shows the frequency spectrum of a dual-tone signal modulated into a bit-stream with a length of 2^{16}. A 114 SNR dB signal can be reconstructed from the bit-stream with proper filtering. Using Eq. 5 and Eq. 6, K and M are found to be 8 and 128, respectively. Using these values, the reconstructed signal has a reduced length of 2^9. The filtered signal's frequency spectrum is shown in the diagram on the right of Figure 6. After decimation, the sampling rate is reduced by 128 times. Hence, the ratio of the signal to sampling frequency ratio is increased by the same amount, which can be observed from diagrams in Figure 6. There is no significant aliasing on the reconstructed signal due to down-sampling, and the SNR of the dual-tone signal is retained at 114 dB.

IV. SIMULATION RESULTS

This section discusses the numerical simulation results presented in [11]. Simulation results in [11] shows that the error of estimating the modulator performance is reduced to a maximum of 3dB from 6 dB as previously reported [10]. The reduced error is attributed to performing analysis and FFT on the filtered modulator output. The filtering makes the analysis more robust to the selection of digitized signal segments. Each segment of a signal has the same length but different starting

point. In [10] FFT and analysis are directly performed on the modulator output and different segment selections of bit-stream would yield different SNRs.

A. Simulation Setup

In the simulation setup, we assume to be testing a second-order delta-sigma modulator with 18-bit resolution, which is equivalent to 110 dB SNR. The theoretical SNR of the signal modulated by a second-order modulator is

$$\begin{aligned} n_o &\approx e_{rms}\frac{\pi^2}{\sqrt{5}OSR^{5/2}} \\ SNR &= \frac{1}{n_o 2\sqrt{2}} \\ &\approx \frac{\sqrt{5}OSR^{5/2}}{2\pi^2\sqrt{2}} \end{aligned} \quad (7)$$

where n_o is the rms of the modulator quantization noise within the signal band, and e_{rms} is the rms of the error introduced at the quantizer

Assuming that e_{rms} is 1 and that the input signal RMS is $1/2\sqrt{2}$, a 110 dB SNR modulator requires an OSR of at least 430 calculated from Eq. 7. In the setup, the OSR is 2^9, which is the next higher integer number to satisfy 2^n, where n is an integer. This number assignment is to ensure fast and accurate analysis when performing FFT.

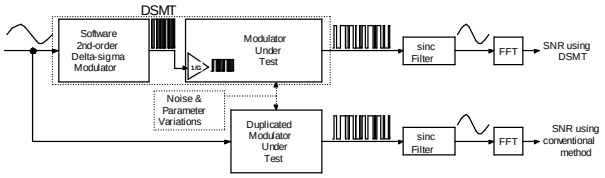

Figure 7 Simulation Setup for Validating the DSMT

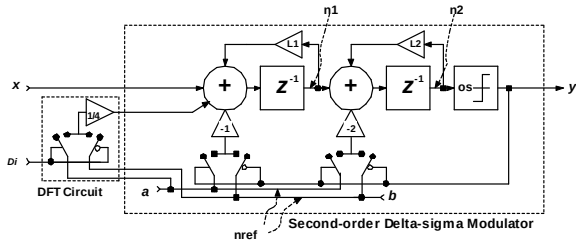

Figure 8 A Non-ideal Model for DfT Modulator

Figure 7 shows the experiment setup while Table 1 shows the parameter settings used in the setup. The sampling frequency of the modulator is set to a unit value while other frequency parameters are referenced to it. The OSR determines the signal bandwidth, f_{BW}, which marks the frequency range bounding the noise components used to calculate the MUT's SNR. The analog stimulus is a dual-tone signal that contains two frequency components – f_1 and f_2. The stimulus is modulated by a software second-order delta-sigma modulator into a digital bit-stream with a length of 2^{16}. The amplitude of the dual-tone stimulus is set to half of the software modulator's input range to ensure stable modulator operation. The digital bit-stream generated by the software modulator is the test stimulus for the proposed DSMT. The amplitude of the digital stimulus is reduced to a quarter ($1/G$) of the modulator input range before it is applied to the MUT. FFT is performed on the MUTs' output, which is filtered by the sinc filter, to determine the modulator SNR. Using Eq. 5 and Eq. 6, the *sinc* filter parameters, K and M, are calculated to be 8 and 128, respectively.

TABLE 1 PARAMETERS FOR SIMULATION SETUP

Setup Parameter	Value
f_s	1
OSR	2^9
f_{BW}	$1/(2\cdot\text{OSR})$
f_1	$2\cdot f_{BW}/2^6$
f_2	$3\cdot f_{BW}/2^6$
G	4
K	8
M	128

Table 2 shows the parameters' boundaries for emulating non-ideal MUTs. Each MUT have parameters' value ($L1$, $L2$, a, b and t) delimited by the boundaries. In addition, noise components $n1$, $n2$, and $nref$, introduce at the outputs of the two integrators and the reference voltages of the MUT, are bounded by their upper limits. Hence, the stimulus to test the modulator is prone to such noise in this experiment setup as depicted in Figure 8. The boundaries are set so that each injected noise or deviated parameters could lower the modulator SNR by a maximum of 10 dB from that of the ideal modulator.

TABLE 2 MUTS' PARAMETERS BOUNDARIES AND NOISE UPPER LIMIT

Parameter	Boundaries
$L1$	0.98 – 1
$L2$	0.98 – 1
A	0.9875 – 1.0125
B	$-a$
T	-0.0125 – 0.0125
$n1$	$1/2^{13}$ (max amplitude)
$n2$	$1/2^5$ (max amplitude)
$nref$	$1/2^{13}$ (max amplitude)

B. Experimental Results

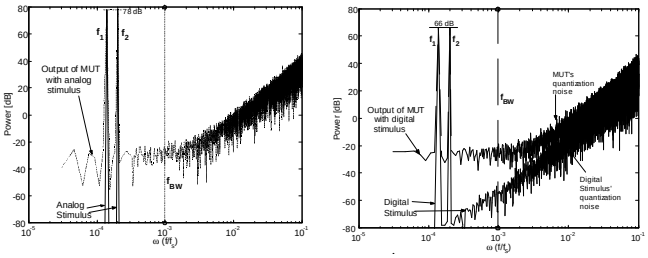

Figure 9 MUT output spectrum with analog and digital stimulus before filtering

This section presents the simulation result of 500 MUTs generated according to the above-mentioned criteria. Diagrams in Figure 9 show the output spectrums of an MUT when its input is applied with the analog and the digital stimulus, respectively. The deviated parameters and the injected noises in the MUT have caused the noise floor in the baseband of the MUT's output spectrums to rise. For an ideal modulator, the output spectrum will have a sloping down noise floor like that of the digital stimulus shown in the diagram on the right of Figure 9. The baseband is determined by the bandwidth, f_{BW} line shown in the figures. The effect of the amplitude reduction in the digital stimulus is already visible through the power reduction of the dual-tone signal from 78 dB to 66 dB as shown in diagrams of Figure 9. The reduced-amplitude digital stimulus not only maintains the stability of the MUT, but also enables us to determine the SNR of the MUT by calculating the power of the MUT's noise floor within the base band. This noise floor is

significantly higher than that of the digital stimulus as shown in diagram on the right of Figure 9.

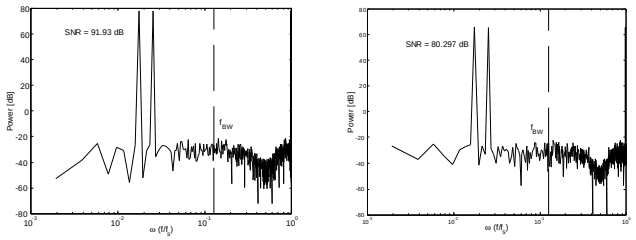

Figure 10 Filtered MUT output spectrum with analog stimulus and digital stimulus

The MUTs' SNR are calculated from the MUT's filtered outputs. The frequency spectrums of the filtered outputs are shown in diagrams of Figure 10. The diagram on the right of Figure 10 shows that the power of the dual-tone signal in the digital stimulus and its corresponding MUT output remains 12 dB less than that in the original analog stimulus, as shown in the diagram on the left of Figure 10. This results in a 12 dB reduction in the SNR when DSMT is used. Hence, an additional 12 dB is added to the MUT SNR when the DSMT is used to perform the measurement.

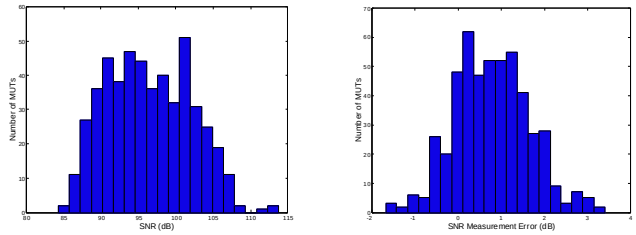

Figure 11 The histograms of the 500 MUTs' SNR and their DSMT SNR measurement error

Diagram on the left of Figure 11 shows the histogram of the 500 MUTs' SNR. These SNRs are calculated using the analog signal as the test stimulus. The 500 SNRs have a mean of 96.5 dB and a standard deviation of 5.6 dB. The SNR of the MUTs ranges from 84.2 dB to 113.8 dB. An ideal MUT has a 114 dB SNR, which is equivalent to that of an 18.7-bit resolution system.

The diagram on the right of Figure 11 shows the Histogram of the DSMT SNR measurement error for the same 500 MUTs. A positive SNR measurement error denotes that the DSMT has overestimated the MUT SNR by the error amount. The measurement errors have a mean of 0.78 dB and a standard deviation of 0.86 dB. The measurement errors range from -1.67 dB to 3.4 dB. A 3 dB is equivalent to a ½ least significant bit (LSB) of the MUT. These figures translate to a maximum measurement error of 0.57-bit resolution for an 18-bit system (110 dB). The results show that the DSMT could closely estimate the performance of the modulator down to a maximum of error of 3 dB.

V. CONCLUSION

In this paper, we have presented a sigma-delta DfT architecture that can be tested with digital signal. This feature removes the needs of generating analog signal, which can be costly for high-resolution modulators. Generating numerous DC levels to test high-resolution modulator is costly and ineffective, as the modulator operation is not test with actual dynamic form of signal. When this DfT modulator is implemented in an SoC platform, it breaks the deadlock commonly found in the mixed-signal BIST architecture where the analog stimulus generator and the analog signal digitizer function inter-dependently in performing self-characterization. In this case, the signal digitizer, a DfT delta-sigma modulator, requires only a digital stimulus to perform characterization. The test time in the DSMT is also significantly shorter than that of the static linear ramp testing, which is the only reported test available for high-resolution ADCs. As mentioned in Section III-C, the DSMT requires only 2^9 samples of filtered signal to analyze an 18-bit modulator, while static test would require at least 2^{18+2} samples of filtered signal.

REFERENCES

1. A. K. Lu and G. Roberts, "An Analog Multi-Tone Signal Generator of Built-in Self-test Applications," In *Proc. International Test Conference*, October 1994, pp. 650–659.
2. X. Haurie and G. Roberts, "Arbitrary-Precision Signal Generation for Mixed-Signal Built-in Self-test," *IEEE Transactions on Circuits & Systems*, 45(11): pp. 1425–1432, November 1998.
3. J.-L. Huang and K.-T Cheng, "Testing and Characterization of the One-Bit First-Order Delta-Sigma Modulator for On-Chip Analog Signal Analysis," In *Proc. International Test Conference*, October 2000, pp 1021–30.
4. J.-L. Huang, C.K. Ong, and K.-T Cheng, "A BIST Scheme for On-chip ADC and DAC Testing," In *Proc. Design, Automation and Test in Europe*, March 2000, pp. 216–220.
5. M. Hafed, N. Abaskharoun, and G. Roberts, "A stand-alone integrated test core for time and frequency domain measurements," In *Proc. International Test Conference*, October 2001, pp. 1190 – 1199.
6. B. Dufort, G. Roberts, "Increasing the performance of arbitrary waveform generators using periodic sigma-delta modulated streams," *IEEE Transactions on Instrumentation and Measurement*, Vol. 49 (1), pp. 188 – 199, February 2000.
7. V. D. Plassche, "*Integrater Analog-To-Digital and Digital-To-Analog Converters*," Kluwer Academic Publishers, Boston, 1994.
8. M.F. Toner and G. W. Roberts, "A BIST Scheme for an SNR Test of a Sigma-delta ADC," In *Proc. International Test Conference*, October 1993, pp 805 – 814.
9. C.K. Ong, J.-L. Huang, and K.-T. Cheng, "Testing Second-order Delta-sigma Modulator Using Pseudo-random Pattern," In *Proc. International Mixed-signal Testing Workshop*, June 2001, pp. 55–71.
10. C.-K. Ong and K.-T. Cheng, "Self-Testing Second-Order Delta-Sigma Modulators Using Digital Stimulus," In *Proc. VLSI Test Symposium*, April 2002, pp. 237 – 246.
11. C.-K. Ong, K.-T. Cheng, and L. Wang, "Delta-Sigma Modulator Based Mixed-signal BIST Architecture for SoC," In *Proc. Asia and South Pacific Design Automation Conference*, January 2003, pp. 669 – 674.
12. S. Norsworthy, R. Schreier, and G. Temes, "*Delta-Sigma Data Converters: Theory, Design, and Simulation,*" IEEE Press, New York, 1996.
13. "Data Converters" http://www.ti.com/sc/docs/products/index.htm
14. "A-to-D" http://www.linear.com/prod/pft.html
15. J. Candy, "A Use of Double Integration in Sigma Delta Modulation," *IEEE Transactions on Communication*, COM-33(3), pp. 249 – 258, March 1985.
16. G. Lainey, R. Saintlaurens, and P. Senn, "Switched-capacitor Second-order Noise-Shaping Coder," In *IEE Electronics Letter*, February1983, pp. 149 – 150.
17. J. Candy and G. Temes, "*Oversampling Delta-Sigma Data Converters: Theory, Design, and Simulation,*" IEEE Press, New York, 1992.
18. O. Feely, "Nonlinear Dynamics of Chaotic Double-Loop Sigma-Delta Modulation," In *Proc. International Symposium on Circuits and Systems*, May 1994, pp. 101 – 104.
19. E. Dijkstra, O. Nys, C. Piguet, and M. Degrauwe, "On the use of modulo arithmetic comb filters in sigma delta modulators," In *Proc. International Conference on Acoustics Speech and Signal Processing*, April 1988, pp. 2001–2004.