A Stereo Multibit ΣΔ DAC with Asynchronous Master-Clock Interface

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***Abstract*—A two-channel multibit ΣΔ audio digital-to-analog-converter (DAC) with on-chip digital phase-locked loop and sample-rate converter is described. The circuit requires no oversampled synchronous clocks to operate and rejects input sample clock jitter above 16 Hz at 6 dB/octave. A second-order modulator with a multibit quantizer, switched-capacitor (SC) DAC, and single-ended second-order SC filter provides a measured out-of-band noise of −63 dBr with less than 0.1° phase nonlinearity. Measured S/(THD + N) of the DAC channel including a 0–63 dB, 1 dB/step attenuator is greater than 90 dB unweighted. The circuit is implemented in 0.6-μm DPDM CMOS, dissipating 220 mW at 5 V. Die size is 3 mm × 4 mm.**

I. Introduction

COMPARED with traditional Nyquist-rate laser-trimmed R-2R digital-to-analog converers (DAC's), oversampling ΣΔ audio DAC's generally offer higher integration, lower cost, freedom from low-level distortion, and reduced analog smoothing filter requirements. One drawback of oversampling DAC's is that a high-frequency synchronous clock, typically between 256–512× the input sample rate, is required to drive the digital interpolation filter and oversampled DAC. Also, when a high SNR is desired, the jitter requirements of this clock are stringent, especially for low resolution (single-bit) DAC's [1]. In applications where the source of digital audio data is remote, such as cable set-top boxes, digital-audio radio broadcast, and digital audio link over a network, this synchronous high-frequency clock is generally not available and must be extracted and synthesized from the audio-data stream. This is often done using an external phase-locked loop (PLL) as part of a clock and data recovery system. A second PLL is sometimes necessary to suppress clock jitter further for applications seeking greater than 100 dB in SNR [3].

Fig. 1 shows a block diagram of a conventional ΣΔ DAC [14], [15]. A PLL derived oversampled clock is used to drive the digital filter, modulator, and a 1-b DAC. The DAC's sensitivity to clock jitter is proportional to the sample-to-sample step size at its discrete-time to continuous-time interface which is related to the amount of out-of-band noise present [2]. In general, higher out-of-band noise implies a larger output slew-rate and also a larger average step-size. For 1-b DAC's, the sample-to-sample step size can be full scale in amplitude. To reduce clock jitter sensitivity, a high-order discrete-time filter can be applied to remove the out-of-band noise [5] or the quantization step size can be made finer by using a multibit DAC [4], [12], [13].

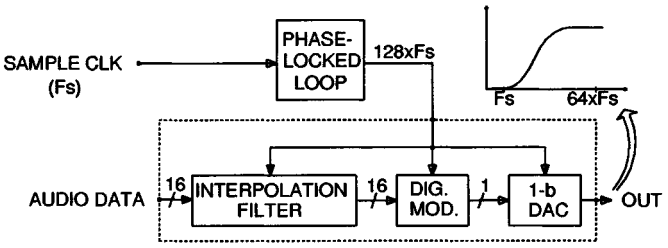

Fig. 1. Conventional ΣΔ DAC interface with synchronous and oversampled clock.

To relieve the system designer from the burden of synthesizing a low-jitter, synchronous, and oversampled clock, an oversampling DAC that requires no synchronous oversampled master clock to operate is described. The DAC features an on-chip digital phase-locked loop (DPLL) and a digital sample-rate converter to decouple the analog DAC's output-rate from the input sample clock rate. This allows the DAC to be driven by an independent low-jitter clock source which minimizes jitter-induced amplitude errors. The DAC uses a second-order digital modulator in combination with a 17-level quantizer to achieve greater than 110 dB theoretical SNR and reduced out-of-band noise when compared with higher-order 1-b modulators. The problem of element matching in a multibit DAC is addressed by using a dynamic element matching technique that shuffles the thermometer decoded outputs of the modulator. The shuffling algorithm in earlier dynamic element matching techniques had been controlled by either a periodic clock [6] or a psuedorandom data stream [9] which modulates mismatch errors into tones and white noise, respectively. The shuffling algorithm presented here is data-directed and results in first-order highpass noise shaping of the element matching error.

II. DAC Overview

Fig. 2 shows a block diagram of the proposed DAC. The DAC uses a DPLL to synthesize an oversampled and synchronous clock from an external asynchronous master clock. This synchronous clock is used to drive an interpolation filter to bring the data rate to 128 times the input rate (F_s). The digital sample and hold (S/H) raises the data rate at the output of the interpolation filter to a fixed rate determined by an

Manuscript received June 18, 1996; revised July 23, 1996.

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Publisher Item Identifier S 0018-9200(96)08217-0.

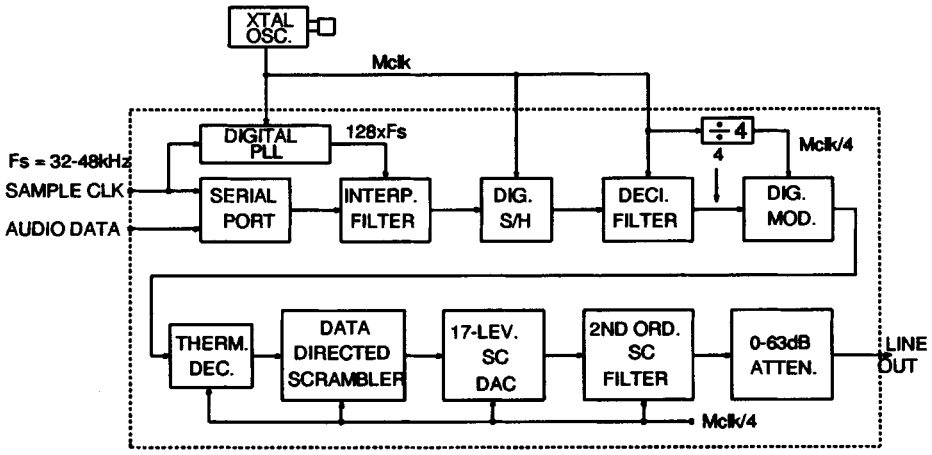

Fig. 2. Proposed $\Sigma\Delta$ DAC with Nyquist-rate interface.

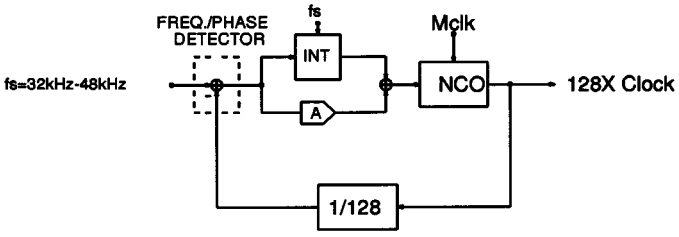

Fig. 3. A block diagram of a digital phase-locked loop.

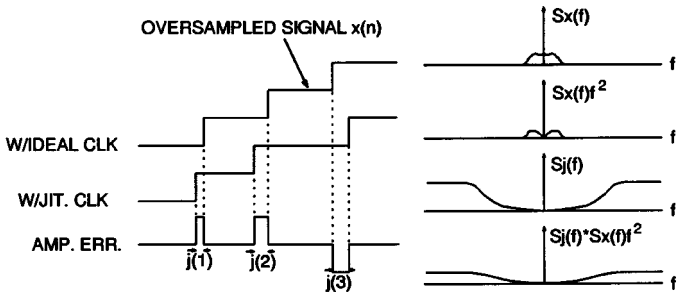

Fig. 4. Effect of DPLL phase errors on interpolator output.

external master clock (M_{clk}). This decouples the input sample rate from the DAC output rate, thus allowing a low-jitter clock (e.g., crystal controlled) to drive the DAC which minimizes jitter-induced DAC noise.

An additional benefit of operating the DAC at a fixed rate is that the DAC conversion rate and out-of-band noise spectrum does not scale with the input sample rate. This is helpful because for conventional "synchronous" DAC's, lowering the input data rate can bring nominally out-of-band noise inside the audioband, especially in applications such as MPEG decoders where a wide range of audio sample-rates are expected.

The highly-oversampled data at the output of the S/H is decimated by four before driving a second-order digital modulator. This lowers the operating speed of the analog circuitry that follows without significantly degrading performance. The multibit output of the modulator is thermometer decoded and scrambled before being fed to a switched-capacitor DAC and filter. A 0–63 dB 1 dB/step attenuator delivering a full scale output of 3 V_{pp} peak-to-peak completes the DAC channel circuitry.

A. DPLL

Fig. 3 shows a block diagram of the DPLL consisting of a frequency-phase detector, proportional plus integral loop filter, and a numerically controlled oscillator (NCO). The DPLL offers dual-loop bandwidths for fast acquisition and jitter-free tracking. Loop bandwidth is determined automatically using the phase detector output. When tracking with the lower bandwidth, the DPLL rejects sample clock jitter noise above 16 Hz which is not often possible with fully integrated analog PLL's. One important drawback of synthesizing a clock using a DPLL is that its output clock edges are fixed by the finite time-resolution of an external master clock that drives its NCO. The synthesized clock can have jitter up to the time-resolution of its master clock (37 ns at 27 MHz).

Fig. 4 illustrates the effect of NCO clock jitter on the interpolation filter output in both time and frequency domain. Let the jitter be defined by $j(n)$. The low-frequency component of the amplitude error at each sample is simply $j(n)$ times the step change from sample to sample. In the frequency domain, the spectral density of the error is proportional to $Sj(f) * Sx(f) \cdot f^2$ where $Sj(f)$ and $Sx(f)$ represent the spectral density of $j(n)$ and input signal and f is the frequency variable. It can be seen from Fig. 4 that if the spectral shape of the jitter is highpass, then the resulting jitter induced amplitude errors will also be highpass in spectrum. By highpass noise-shaping the jitter spectrum, signal quality in the audio band can be preserved.

Based on simulations, second-order highpass noise-shaping of the NCO jitter is sufficient to preserve 16-b quality (effective number of bits) for a full scale 20 kHz sinewave sampled at 48 kHz. To synthesize a clock whose jitter is second-order noise-shaped, a second-order digital modulator shown in Fig. 5 is used [7]. Given the input to the modulator is a dc signal representing the desired output period, traditional $\Sigma\Delta$ theory

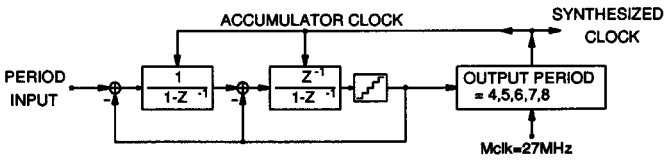

Fig. 5. A numerically-controlled oscillator whose jitter is second-order high-pass noise-shaped.

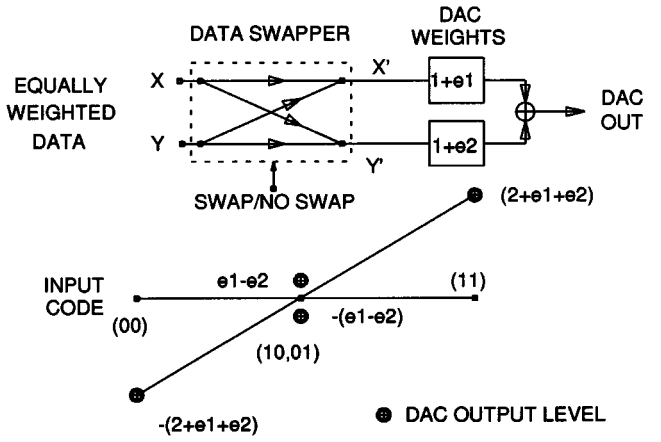

Fig. 6. A block diagram of a three-level DAC with a data swapper and its transfer function.

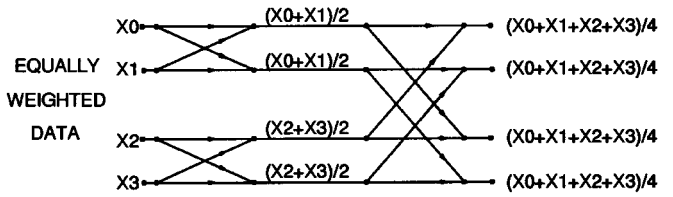

Fig. 7. A four-element butterfly data-directed scrambler showing signal weights at each node.

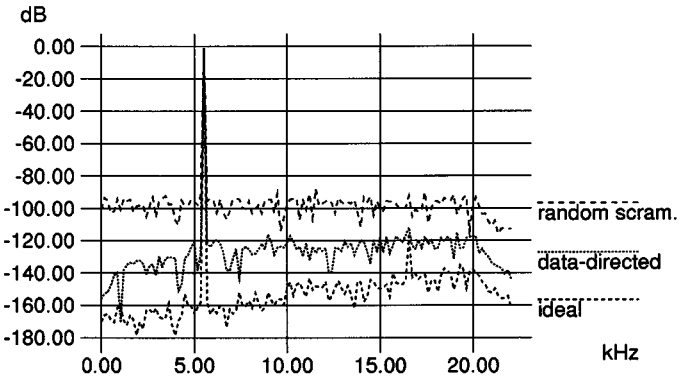

Fig. 8. FFT's of simulated DAC output for the cases of random scrambling, data-directed scrambling, and ideal matching.

predicts the output of the quantizer is a sequence of numbers that represents the desired period but with the addition of second-order highpass shaped noise. The programmable divider at the output of the quantizer accepts this sequence of noise-shaped numbers and generates a clock whose sequence of periods are a scaled (by M_{clk}) version of its input. Thus the jitter in the resulting synthesized clock shares the same spectral shaping as one would expect of the quantization error from a second-order modulator.

Given a master clock frequency of 27 MHz and a programmable divider with a divide ratio from four to eight, the DPLL can track input frequencies from 26–52 kHz which covers the popular digital audio sample-rates of 32, 44.1, and 48 kHz.

B. Variable-Rate Digital Interpolation Filter

The interpolation filter is implemented using shift-and-add hardware described in [11] which eliminates the need for a multiplier. The filter function consists of a droop equalizer, two halfband filters, and a linear interpolator to bring the rate to 128 times the input rate. The halfband filter's coefficients are derived and quantized into canonical sign digit format using a filter design program provided by Lim [10]. The program optimizes the total number of shift-and-add operations while minimizing frequency response degradation due to coefficient quantization. A digital sample-and-hold is used to bring the data rate to the master clock frequency of 27 MHz independent of the input sample rate. A decimation filter drops the data rate by 4–6.75 MHz to reduce the operating speed of the SC DAC and filter.

The interpolation filter response has a ripple of 0.07 dB and a stopband attenuation of 63 dB. It requires 250 shift-and-add operations per input sample which implies only one adder is needed per channel.

C. Data-Directed Scrambling for Multibit DAC's

A multibit noise shaper has the advantages of unconditional stability, higher SNR for a given order, wider usable input range before overload, and lower out-of-band noise. In the past, these benefits have been outweighed by severe linearity requirements for a multibit DAC. In this circuit, the DAC employs 16 equally weighted switched-capacitor elements providing a resolution of 17-levels. The equally-weighted DAC data is scrambled in a data-directed manner which provides first-order highpass noise-shaping of the capacitor mismatch errors [8].

The operation of the scrambler can be best explained by starting with a three-level DAC. Fig. 6 shows a three-level DAC with weights $1 + e1$ and $1 + e2$ where $e1$ and $e2$ are mismatch errors. Assuming a reference voltage of 1 V, the four possible analog output levels for any binary code are $2 + e1 + e2$, $-(2 + e1 + e2)$, $e1 - e2$, and $-(e1 - e2)$, all in volts. If the gain error is ignored, then the midpoint is the only source of nonlinearity in the transfer function as shown in the bottom of Fig. 6. A DAC error is made when data for the two elements is different.

The sign of these errors can be controlled by dynamically "swapping" the two inputs to the DAC. Since an error is made only when the two inputs are different, the long-term error can be forced to zero by alternating the sign of these errors. Simulations show that in addition to eliminating the dc

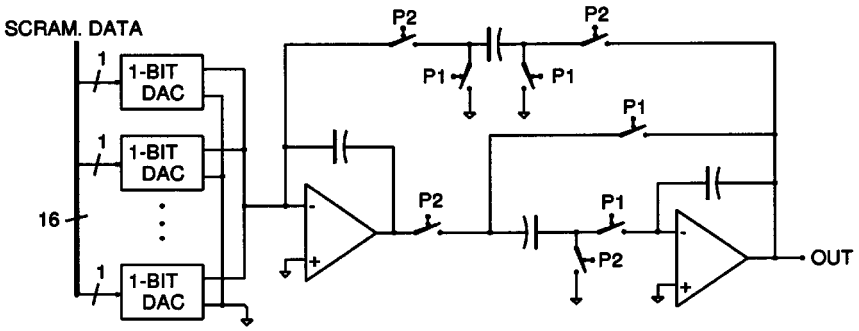

Fig. 9. A schematic of a multibit DAC and second order filter.

TABLE I
STATE TRANSITION TABLE FOR SWAPPER LOGIC; X AND Y ARE SWAPPER INPUTS

X Y	Present State	Next State	Action
00	Even	Even	Don't Care
00	X ahead	X ahead	Don't Care
01	Even	X ahead	Swap
01	X ahead	Even	No Swap
10	Even	X ahead	No Swap
10	X ahead	Even	Swap
11	Even	Even	Don't Care
11	X ahead	X ahead	Don't Care

TABLE II
SIMULATED PERFORMANCE OF A SECOND-ORDER MULTIBIT MODULATOR

Condition	Inband SNR
Ideal matching	116.5dB
1% RMS error Random Scrambling	75.6dB
1% RMS error Data-directed	101.8dB

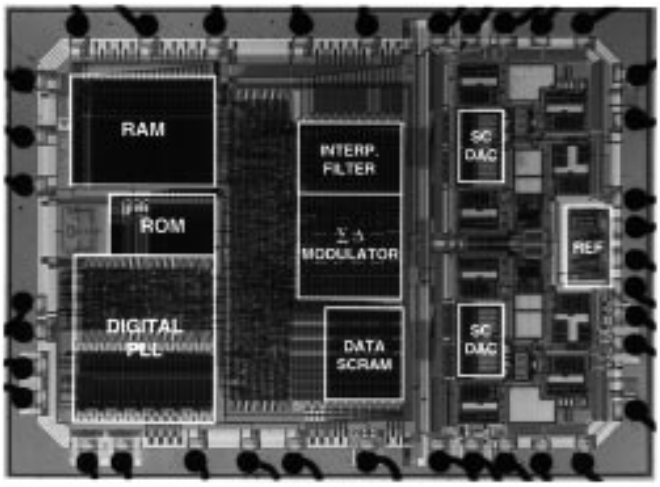

Fig. 10. Chip microphotograph.

error, the noise from element-mismatch errors is shaped by a first-order highpass function.

A different view is to consider the signals at the swapper outputs X' and Y'. A simple decoding scheme for dc signals is to count the number of "1" data values arriving at X' and Y' and normalize the count over time. Because of the swapping action, the "1" data counts between X' and Y' can only differ by one count or less. This implies over time the dc content of X' and Y' converges to the same value which is equivalent to $X' = (X + Y)/2$ and $Y' = (X + Y)/2$. The DAC 's dc output is now given by $(X + Y)(2 + e1 + e2)/2$ with the mismatch errors affecting the gain but not the linearity of the DAC. This analysis is exact for dc signals and will degrade as the frequency of the signal is increased.

Table I shows the state transition table for the logic that controls the swapper. Signals X and Y represent the swapper inputs. The swapper control logic can be implemented using one flip-flop and two exclusive-or gates.

Fig. 7 shows how a DAC with more than two levels can be constructed from the basic two-in two-out swapper cell of Fig. 6. This configuration was originally disclosed by Carley [9] for randomization of the mismatch noise. When the swapper cell is data-directed as previously described, the mismatch noise of the entire system becomes highpass in nature.

The effect of DAC mismatch errors on inband SNR is simulated by introducing a fractional rms mismatch of 1% in the DAC elements. Table II tabulates the simulated inband SNR's for a second-order modulator operating at $128 \times F_s$ under the condition of ideal matching, random scrambling with 1% mismatch error, and data-directed scrambling with 1% mismatch error. Fig. 8 shows fast Fourier transforms (FFT's) of the simulated DAC output for the above conditions.

D. Switched-Capacitor Smoothing Filter

The multibit DAC is followed by a second-order switched-capacitor (SC) filter designed to a thermal noise target of -103 dBr, corresponding to a total input capacitance of 2.4 pF. Fig. 9 shows a schematic of the 17-level DAC and switched-capacitor filter. The SC filter is implemented with single-ended circuitry to minimize area and to simplify the analog interface since consumer audio equipment typically accepts only single-ended signals. The -3 dB filter bandwidth of the filter is greater than 100 kHz for a sample-rate of 6.75 MHz. The high cutoff frequency together with a designed filter Q of 0.5 ensures less than 0.1° of phase nonlinearity over 20 kHz. The SC filter in combination with the second-order multibit modulator achieves a total out-of-band noise figure of

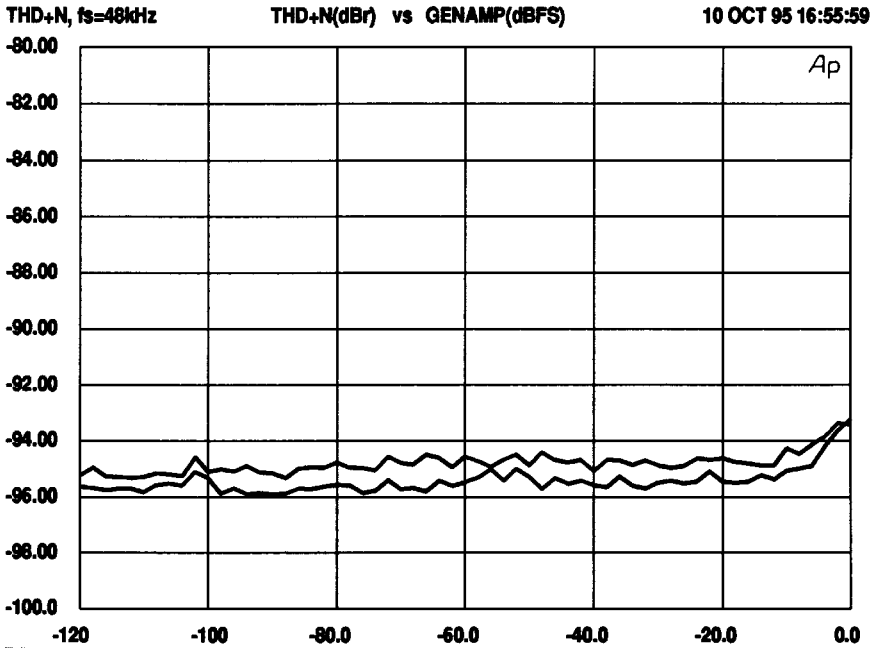

Fig. 11. Measured THD + N versus amplitude, input frequency is 1 kHz/10 kHz (top/bottom trace).

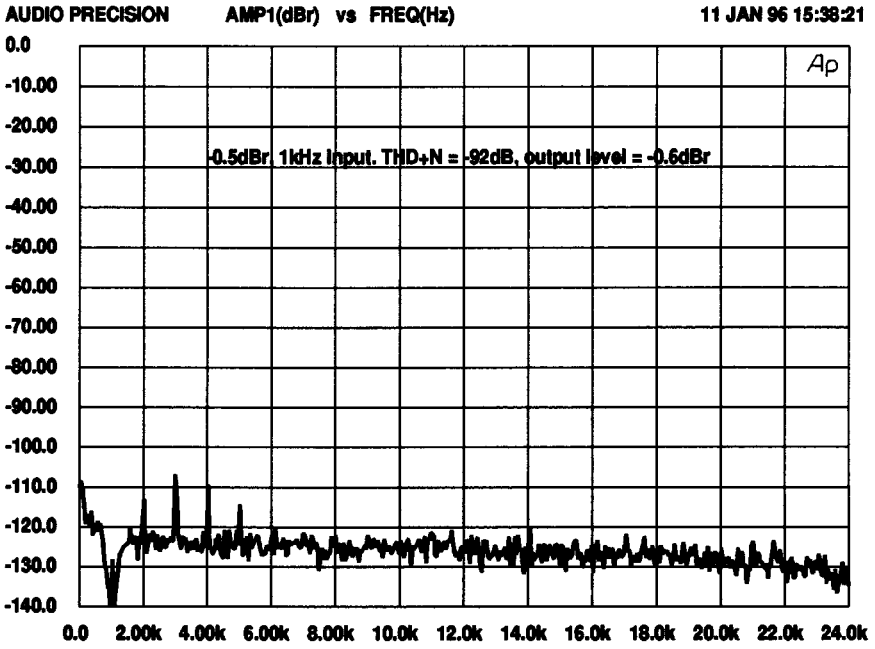

Fig. 12. A 4096-point FFT of the measured DAC THD + N, input level/frequency is −0.5 dBr/1 kHz.

−63 dBr. In addition to the SC filter, a 0–63 dB (1 dB/step) attenuator with separate serial interface is also integrated to form a complete audio processor.

III. Measured Results

Fig. 10 shows a microphotograph of the DAC. Dimensions are approximately 3 mm × 4 mm in 0.6-μm, double-poly, double-metal CMOS. The data-directed scrambler area overhead is 600 μm× 500 μm.

All measured results below are from an Audio Precision System One Analyzer. Fig. 11 plots measured distortion and noise (THD + N) versus input amplitude for signals with input frequencies of 1 kHz and 10 kHz, both sampled at 48 kHz. Fig. 12 shows an FFT of the DAC's measured THD + N. The input sample rate is 48 kHz and the DAC output conversion rate is 6.75 MHz. The input level is −0.5 dBr and the fundamental has been removed with an analog notch filter to lower the dynamic-range requirement for the analog-to-digital converter making the measurement.

To test the data-directed scrambler under large mismatch errors, one of the 16 DAC capacitors in the DAC channel measured above is removed via a laser cut. Fig. 13 shows an

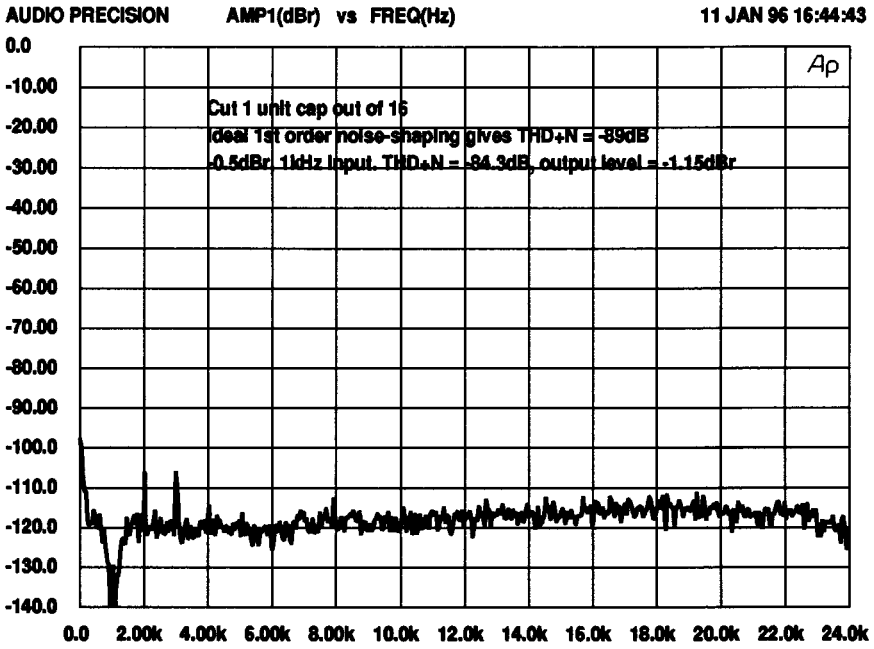

Fig. 13. A 4096-point FFT of the measured DAC THD + N after one of the 16 DAC capacitors has been removed, input level/frequency is −0.5 dBr/1 kHz.

TABLE III
CHIP SUMMARY

Output level	3 Vpp
THD+N (18-bit, -10 dB signal, 22 kHz BW)	-95 dBr
THD+N (18-bit, -0.5 dB signal, 22 kHz BW)	-93 dBr
Total out-of-band noise	-63 dBr
Phase non-linearity, 0-20 kHz	< 0.1°
Input sample-rate lock range @ Mclk = 27 MHz	26-52 kHz
Power dissipation @ 5V, Mclk = 27 MHz	Analog 130 mW
	Digital 90 mW
Maximum clock frequency @ 5V	> 35 MHz
Technology	0.6μm DPDM CMOS
Chip size	3 mm x 4 mm

FFT of the DAC's THD + N output. Assuming the spectrum of the mismatched error is white, the theoretical THD + N is −89 dBr given ideal first-order noise shaping. This figure does not include other noise and error sources. The actual measured THD + N is −84.3 dBr. The highpass noise shaping of the noise floor is evident. The roll-off beyond 22 kHz is due to the Audio Precision's internal band-limiting filter. Table III gives a summary of the DAC's characteristics.

IV. CONCLUSION

The requirement for a synchronous oversampled clock in an oversampled $\Sigma\Delta$ DAC has been eliminated by using a digital PLL. The decoupling of the DAC's input and output sample clocks using a sample-rate converter enables the use of a local low-jitter clock for D/A conversion. Higher inband SNR and lower out-of-band noise is realized by using a multibit quantizer for a second-order modulator. Element matching requirements in the multibit DAC are alleviated by using a data-directed scrambling technique. Experimental results show that an S/(THD + N) of greater than 90 dB is achievable.

ACKNOWLEDGMENT

The authors thank K. Sweetland and D. McNamara for mask design, M. Mueck and P. Ferguson for discussion and insights, and S. Roy and L. Long for testing and support.

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