A Multibit Delta–Sigma Audio DAC with 120-dB Dynamic Range

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***Abstract*—A 24-bit 192-kHz sample-rate digital-to-analog converter (DAC) achieves 120-dB A-weighted dynamic range in the 20-kHz band, and consumes 310 mW with a 5-V power supply. A third-order five-bit $\Delta\Sigma$ architecture optimized for high-end consumer audio has been developed and used. A switched-capacitor (SC) DAC combined with infinite-impulse response (IIR) and finite-impulse response (FIR) filters is employed to increase immunity to clock jitter, and reduce analog power. Partial-range dynamic element matching (DEM) enhances mismatch shaping with reduced circuit overhead. The 7.8-mm^2 chip fabricated in 0.5-μm CMOS integrates a stereo DAC and all functions required for DVD-audio playback.**

***Index Terms*—Delta–sigma modulation, digital–analog conversion, operational amplifiers, switched-capacitor circuits.**

I. Introduction

DVD-AUDIO is a high-quality audio standard that supports 24-bit linear pulse-code modulation (PCM) with sampling rates as high as 192 kHz.[1] The growth of DVD-audio has increased the demand for an audio digital-to-analog converter (DAC) that meets the low-cost needs of consumer applications and achieves the wide dynamic range and high linearity required for professional use [1]. In addition to a cost-effective die size, there are several key requirements for such consumer high-end audio DAC's. First, dynamic range over 115 dB is required using only a 5-V power supply. Secondly, the DAC must tolerate clock jitter of commercially available audio interface IC's. Thirdly, power dissipation should be small enough to house a stereo implementation in a small, low-cost plastic package. With a thermal resistivity of 90 °C/W (typical of a 28-pin VSOP), and maximum junction temperature of 125 °C, power dissipation must be lower than 610 mW for operation in the 0 ° to 70 °C temperature range. Finally, input sample rates f_s of 96 kHz and 192 kHz must be supported in addition to the standard 48 kHz rate. Previous consumer high-end solutions either require an off-chip I/V converter [2], or do not support the 192-kHz sample rate [3]. This paper describes the development of a multibit delta–sigma ($\Delta\Sigma$) DAC that fulfills the above demands.

Multibit $\Delta\Sigma$ modulation offers several features for audio digital-to-analog conversion. In audio, the performance at a very small signal level such as -60 dB relative to full-scale (dBr) is important. As shown in Fig. 1, in conventional 1-bit quantization, the output data toggles between plus and minus full-scale even for a small level signal, generating large quantization noise. In case of multibit quantization using an odd level quantizer (i.e. 15 levels instead of 16), the output will be mainly the midscale zero code, with occasional plus and minus LSB's. This reduces the amount of quantization noise and also the number of the output code transitions. As a result, both idle pattern tones and clock jitter sensitivity are reduced. Also, analog post filtering requirements are relaxed, because of the smaller out-of-band quantization noise. The disadvantage of multibit quantization is the necessity of dynamic element matching (DEM) to correct nonlinearity in the internal multibit DAC.

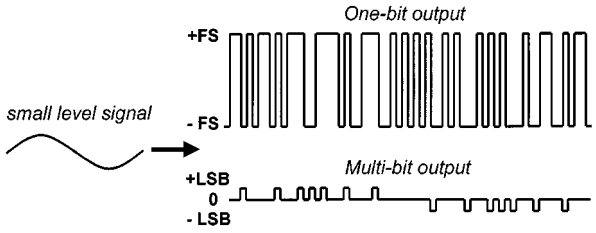

Fig. 1. Advantages of multibit quantization in audio.

Realization of the performance goals involves both architectural and circuit level considerations. On the architectural side, a multibit $\Delta\Sigma$ architecture optimized for high-end consumer audio has been developed. Key issues include system level optimization for clock jitter tolerance, and minimization of circuit overhead required for the DEM, which are discussed in Section II. At circuit level, the key consideration is the power efficiency in analog design for achieving low noise and high linearity. For this purpose, a low-power switched-capacitor (SC) multibit DAC combined with a hybrid post filter has been developed, which is described in Section III. Using these design techniques, a stereo audio DAC with all filtering functions required for DVD-audio playback has been developed in 0.5-μm CMOS. The DAC achieves 120-dB A-weighted dynamic range in the 20-kHz band, and consumes 310 mW of power with a 5-V power supply. General implementation considerations and chip layout of this audio DAC are covered in Section IV. Measured performance and conclusions follow in Sections V and VI.

II. Multibit $\Delta\Sigma$ DAC Architecture Level Design

Fig. 2 shows the signal flow diagram of the multibit $\Delta\Sigma$ DAC for an input sample rate of $f_s = 48$ kHz. The 24-b digital input is first interpolated by $128\times$, and then applied to the digital $\Delta\Sigma$ modulator ($\Delta\Sigma$M) operating at 6.144 MHz. A third-order

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[1]DVD-Audio Version 1.0 Specifications, DVD Forum, October 1998.

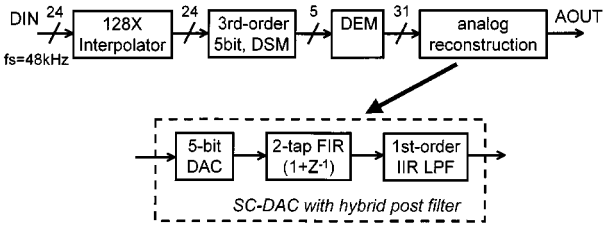

Fig. 2. Multibit delta–sigma DAC signal flow diagram.

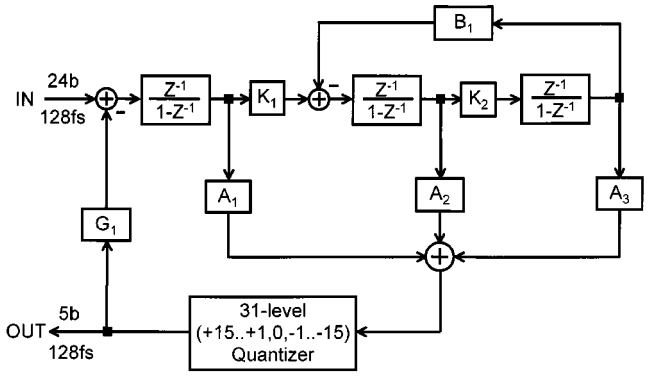

Fig. 3. Digital delta–sigma modulator architecture.

5-b $\Delta\Sigma$M at 128$\times$ oversampling ratio makes theoretical inband quantization noise negligible within the overall noise budget. The digital $\Delta\Sigma$M architecture [4] is shown in Fig. 3. The 5-b $\Delta\Sigma$M output is converted to a 31-level thermometer code, and then DEM processed. The DEM data are fed to the analog reconstruction block, which includes the 5-b DAC and post filtering functions. The analog power supply is 5 V, while the digital operates at 3.3 V to reduce digital switching noise.

A. Clock Jitter Immunity

The main concern at system level design is clock jitter tolerance. In a $\Delta\Sigma$ DAC, clock jitter is translated to noise at the discrete-to-continuous-time interface [5]. Modulation by jitter will fold down the high frequency quantization noise and/or raise the noise spectra at side-bands of the fundamental signal [4]. For a small level signal, the first mechanism is responsible for inband noise performance degradation. Therefore, the amount of high-frequency quantization noise affects the jitter sensitivity. The two possible approaches to reduce high-frequency noise are to increase the quantizer resolution, or to provide more out-of-band filtering in discrete domain. Optimization at the system level involves a compromise between these two key factors. A higher quantizer resolution increases the DEM processing circuit size. On the other hand, more complex filtering increases the analog power dissipation. The design goal for jitter tolerance is to achieve a signal-to-noise ratio (SNR) of 120 dB with a clock jitter of 200-ps rms. This is the worst-case jitter performance of an industry standard audio receiver IC [6]. With a 7-b quantizer, no discrete-time filtering is required to achieve the specification, but DEM decoding of 128 levels will result in a large circuit overhead. With a 5-b quantizer, the DEM size becomes approximately six times smaller (assuming implementation of the data weighted averaging (DWA) [7] algorithm using a barrel shifter). However,

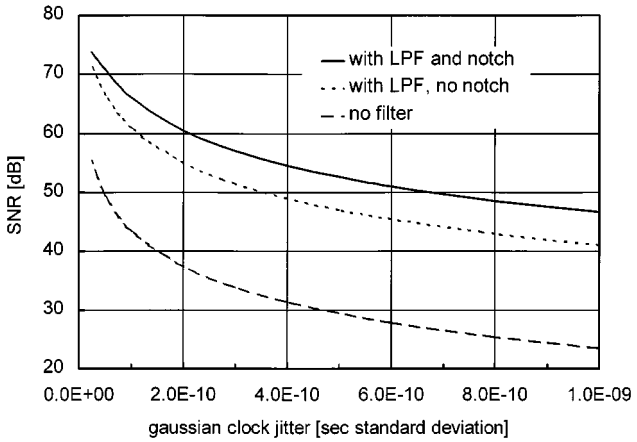

Fig. 4. Simulated SNR versus clock jitter for a -60 dBr 1-kHz signal.

with 5-b quantization a second-order low-pass filter (LPF) is required, which uses two opamps in a conventional SC implementation [8].

In order to provide the necessary filtering for jitter tolerance with a single opamp, a hybrid FIR/IIR filter approach is employed in this design [9]. As described in Fig. 2, a two-tap FIR filter with $1+z^{-1}$ transfer function and a first-order IIR filter are combined. The two-tap FIR filter effectively reduces high-frequency quantization noise by adding a notch at half the oversampling frequency, hence reducing quantization noise modulated back to inband. Since FIR structures do not employ feedback as in IIR structures, no extra opamp is needed. In addition, using the particular SC scheme of this design, both filters can be incorporated into the multibit DAC with almost no increase in power. Circuit design of the 5-b SC DAC with the hybrid filter is discussed in Section III. Fig. 4 shows simulated SNR versus clock jitter for a $\Delta\Sigma$ DAC using 5-b quantization with the hybrid post filter. The signal is 1 kHz at -60 dBr. The simulation includes the theoretical quantization noise of the $\Delta\Sigma$M and any excessive noise caused by clock jitter. With Gaussian clock jitter of 200 ps rms, the SNR without any discrete-time filtering is 98 dB relative to a full-scale signal. Use of a first order LPF with a cut-off frequency of 220 kHz gives an 18-dB improvement in SNR. Addition of the notch filter at 3.072 MHz adds another 6-dB increase, raising the SNR to 121 dB. Here, this hybrid filter allows the use of an area efficient 5-b quantizer without increasing the analog power dissipation.

B. Dynamic Element Matching (DEM)

The drawback of multibit quantization is the nonlinearity of the internal DAC, which is commonly corrected by DEM techniques. The goal of this design is to make element mismatch noise negligible with minimal DEM circuit overhead. The entire noise budget should be allocated to random analog noise sources (kT/C noise and $1/f$ noise), because they directly relate to component sizes and power dissipation. DWA is a common algorithm choice for DEM because of the first-order mismatch shaping and its simplicity in implementation [7]. In DWA, the element selection is rotated sequentially depending on the weighting of the input data. The rotation action over series of samples will result in more averaging for mismatch-in-

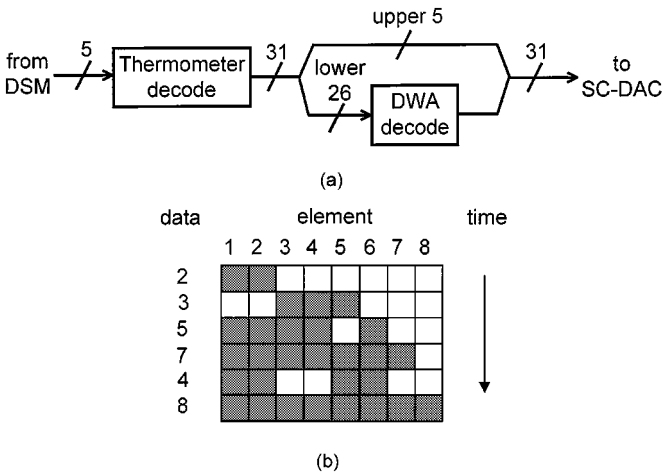

Fig. 5. Partial DWA concept. (a) Block diagram. (b) Operation (3-b DAC example).

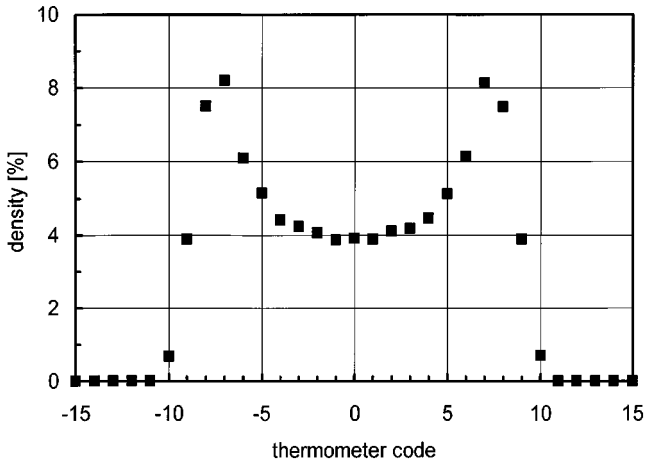

Fig. 6. Thermometer code density for a 1.5-kHz full-scale signal.

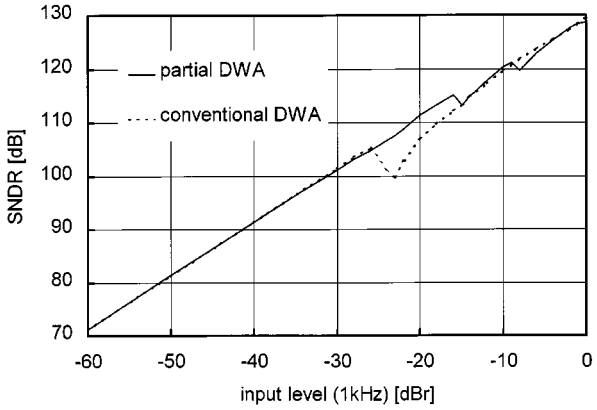

Fig. 7. Simulated SNDR versus input level for a 5-b DAC with 0.2% mismatch.

duced noise with lower frequency components. A disadvantage of DWA is the loss of efficiency for higher DAC resolution. This is because with more DAC levels, each element will be used less frequently, thus reducing the averaging effect [7]. Also, in a SC DAC where the total capacitance is determined by kT/C noise constraints, increase of resolution will reduce the unit size of capacitor elements, and hence degrade element mismatch. In this design, these problems are overcome by performing DWA only partially within the full-scale range. Mismatch-shaping algorithms with second-order or higher [10] were not considered, because of the large circuit overhead.

A conceptual block diagram of the proposed partial-DWA scheme is shown in Fig. 5(a). Within the 31-level thermometer code (-15 to $+15$), only the lower 26 levels (-15 to $+10$) are processed by DWA before controlling the corresponding DAC elements. The upper five levels ($+11$ to $+15$) are fed directly to the DAC. Fig. 5(b) shows the element rotation sequence of partial-DWA using a 3-b (8-level) DAC example. In this case, DWA is performed partially within the lower six elements. In DWA, the efficiency of mismatch averaging is determined by the velocity of rotation, in other words, by the frequency of each element used. In this application, the signal distribution is centered at mid-scale level (± 0). This implies that an average of 16 elements out of 31 is turned on every sample. Conventional DWA rotates within the full range of 31 elements, which means each element is used at an average rate of $16/31$ times-per-sample. In partial-DWA, the velocity is increased because of rotation within 26 elements instead of 31. For thermometer codes up to $+10$, each element is used $16/26$ times-per-sample, hence mismatch averaging is enhanced. For codes above $+10$, the 31-level data fed to the DAC is identical to the thermometer code. The absence of mismatch averaging at large signal levels is of little consequence in this design. Audio signals typically have gaussian distributions where large codes occur less frequently. Furthermore, gain scaling is used in the $\Delta\Sigma$M to avoid overload [4], which further reduces the occurrence of codes near full-scale. The gain scaling is implemented by insertion of gain G_1 as in Fig. 3. A simulated histogram of the thermometer code density for a full-scale 1.5-kHz sinewave is shown in Fig. 6. The occurrence of codes outside the range is approximately 0.04%. Apparently, the histogram may suggest performing partial-DWA in a range centered at midscale, as for levels $+10$ to -10, but this will actually reduce the efficiency. In this case, the five elements corresponding to the lower five levels (-15 to -11) are constantly turned on. The remaining 11 elements will rotate within 21 elements, resulting in a velocity of $11/21$ times-per-sample, which is lower than the proposed scheme of Fig. 5(a).

Fig. 7 contrasts conventional and partial DWA. The signal-to-noise plus distortion (SNDR) was simulated versus input level for a 1-kHz signal. Results for 20 different sets of 5-b DAC's with 0.2% (1σ) gaussian mismatch were averaged to highlight the difference between the two methods. Analog noise sources were not included in the simulation. The sharp dips in the traces are typical artifacts of DWA. Because of the periodic nature of DWA, the shaped mismatch error appears as tones. These out-of-band tones may fold back to inband due to $\Delta\Sigma$ limit cycles that are dependent on the signal level, and degrade the inband SNDR [7]. The signal level where the dip occurs varies with the DAC resolution, and the dip will become deeper with higher resolution. Conventional DWA dips to 100-dB SNDR at -22 dBr, equivalent to 122-dB SNDR for a full-scale signal. Partial DWA improves this to a worst case of 128 dB, making the effect of tones negligible. Setting the partial DWA range to 26 levels makes the SNDR at full-scale 3-dB worse than conventional DWA. The standard deviation is 1.6 dB. This has neg-

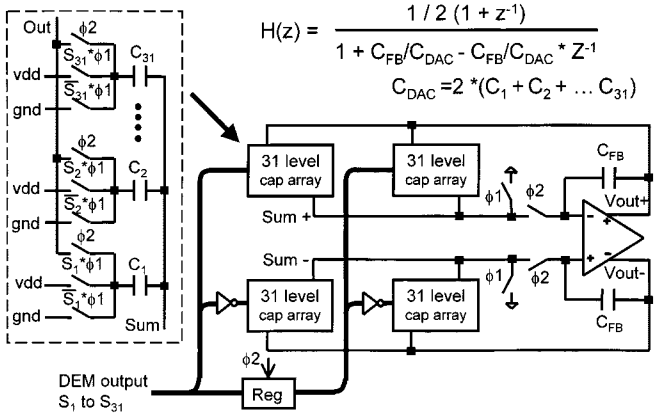

Fig. 8. Five-bit SC DAC with hybrid post filter.

ligible influence to the overall SNDR performance of the ADC, because the distortion caused by analog imperfections becomes dominant at full-scale. The simulation results show that efficiency of DWA can be enhanced by this simple modification. This scheme also reduces the DEM overhead because of the smaller range of data to be decoded.

III. Low-Power SC DAC with Hybrid Post Filter

The major concern in analog design is the architecture of the multibit internal DAC and post filter. In a prior high-end design, a current-mode DAC with continuous-time filtering has been used because of the power savings compared to SC circuits [11]. This approach is more sensitive to clock jitter because of the absence of discrete-time filtering. Either increase of quantizer resolution or additional discrete-time filtering is required to reduce the step size prior to the discrete-to-continuous-time boundary. A SC implementation is less sensitive to clock jitter [12], but the large power caused by kT/C noise constraints makes a conventional SC DAC impractical in high-end designs. This design employs the direct charge transfer (DCT) technique, where a common SC is used for input sampling and feedback [13]. A multibit DAC implementation using this technique makes the slew component of the sampling capacitors negligible, resulting in output drive requirements comparable to continuous-time implementations [4]. In addition, the DCT technique allows the hybrid filter mentioned in Section II-A to be combined with the multibit DAC function using a single opamp with minimal area and power overhead.

The 5-b SC DAC with hybrid post filter is shown in Fig. 8. The fully differential circuit operates at a clock rate of 6.144 MHz. Each capacitor array consists of 31 unit capacitors, C_1 to C_{31}. During the sampling phase $\phi 1$, they sample either VDD or GND depending on the corresponding input data S_1 to S_{31}. During the integrate phase $\phi 2$, all capacitors are connected in parallel between the summing node and opamp output. The output level is generated passively by distributing the charge in the feedback path. At the discrete-to-continuous-time interface of a SC circuit, the distortion performance is determined by the nonlinearity of the whole area under the stair-step waveform, instead of only the final value at the end of the clock phase. The nonlinearity consists of opamp slew-rate limiting, signal-dependent charge injection, and signal-dependent *RC* time constant of the settling curve. The DCT scheme eliminates spikes generated by slew-rate limiting. Four-phase nonoverlap clocks with delayed bottom plate switching are used to reduce the effect of charge injection [13]. The on-resistance variation of the switches connected to the output make the *RC* settling time constant signal dependent, and hence generate distortion. CMOS transmission gates with low-threshold (± 0.3 V) transistors are used to reduce the variation by 40% compared to normal-threshold (± 0.8 V) transistors.

Each half of the differential circuit has two capacitor arrays. One is controlled by the DEM output data, and the other by data delayed one cycle. This realizes the two-tap FIR filter with $1 + z^{-1}$ transfer function. Since the total sampling capacitance $C_{\rm DAC}$ is determined by kT/C noise, there is no power increase by splitting $C_{\rm DAC}$ into two arrays. The only area overhead is the 31-b registers. The feedback capacitor $C_{\rm FB}$ provides a first-order LPF function. The cut-off frequency is 220 kHz, which is determined by the ratio between $C_{\rm FB}$ and $C_{\rm DAC}$. The total $C_{\rm DAC}$ capacitance of 32 pF gives a kT/C noise power in the 20-kHz bandwidth of -119 dB relative to a full-scale sinewave. Because of the direct charge transfer, $C_{\rm DAC}$ does not directly appear as a load to the opamp. The main load capacitance becomes the bottom plate capacitance of $C_{\rm FB}$ and $C_{\rm DAC}$, which is 15 times smaller than intentional circuit capacitance in this fabrication process. As a result, the internal SC sizes have minor influence on the power dissipation. Instead, the power of the opamp is determined by output drive requirements, because the SC DAC directly drives the external circuitry of the audio DAC.

A. Opamp Design

The requirement for the opamp is distortion less than -100 dB with a 2.5-$V_{\rm pp}$ swing into a 600-Ω load. Also, adequate settling of the SC circuit must be achieved with a 50-pF load. A three-stage opamp with a folded cascode input stage and a push-pull output stage [14] was found optimal for high linearity with this load condition. A two-stage implementation was not considered because of the insufficient open-loop dc gain. A dc gain over 100 dB is required to suppress the nonlinearity of the output stage. Fig. 9(a) shows the opamp block diagram. High gain implemented in the folded-cascode stage allows use of low-gain second stages, and still meet the total dc gain target. In the push-pull output stage, relatively large quiescent current is used to ensure stability and low-distortion drive capability. An error feedback from the output to second stage [15] was not employed because of the moderate output swing requirement.

As shown in Fig. 9(b), the nominal output quiescent current I_Q is 6 mA, which makes the output stage source current $I_{\rm PUSH}$ and sink current $I_{\rm PULL}$ vary by only $\pm 20\%$ across the output swing range. This rather "soft" push-pull arrangement without aggressive quiescent current scaling was found beneficial for high linearity. In this implementation, neither the output pMOS driver nor the nMOS driver enters triode region at full-scale swing, eliminating crossover distortion. Also, variation of the parasitic pole positions associated with the output-stage transconductance g_m is minimized. This variation may cause ringing in the SC settling at voltage swings with insufficient

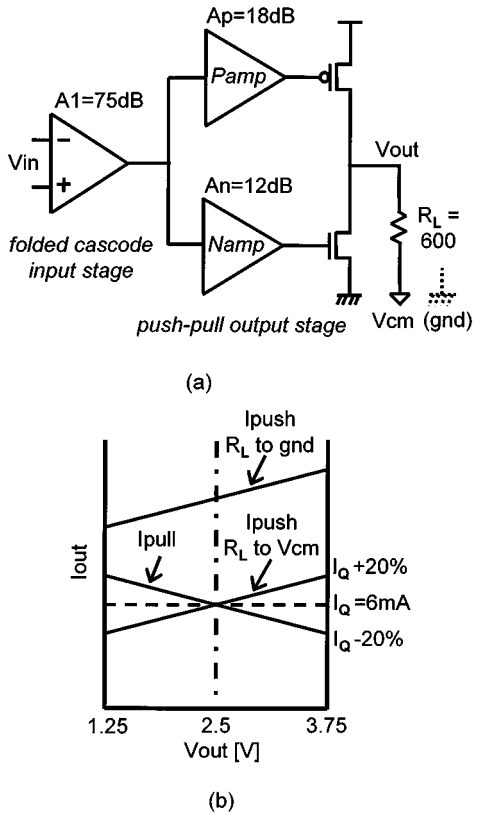

Fig. 9. (a) Three-stage opamp block diagram. (b) "Soft" push-pull concept.

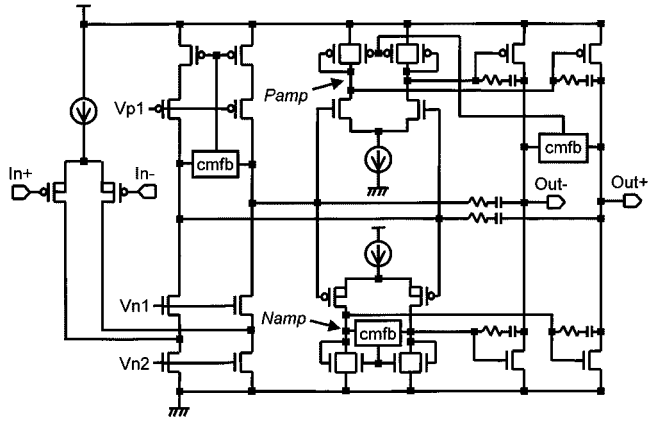

Fig. 10. Opamp circuit diagram.

phase margin, which results in signal-dependent settling inaccuracy, and hence generate distortion. In addition, no extra circuitry for precise control of the quiescent current is required. One unique requirement in this application is that load resistance R_L may be referred to GND instead of VCM (half VDD). To accommodate this, the gain of the pMOS side second-stage amplifier $P_{\rm amp}$ is set 6 dB higher than the nMOS side amplifier $N_{\rm amp}$. If R_L is connected to GND, the extra gain of $P_{\rm amp}$ forces $I_{\rm PUSH}$ to mainly compensate the increase of source current, leaving $I_{\rm PULL}$ almost unchanged. This maintains linearity of the output nMOS driver and prevents increase of distortion.

The circuit diagram of the opamp is shown in Fig. 10. Fully differential circuits are used throughout the signal path, for better rejection of digital switching noise coupled to the substrate. Three common-mode feedback (CMFB) loops independently control the output common-mode voltage of three different stages. Each CMFB consists of a divider circuit and an auxiliary amplifier (differential pair). In the first stage and $N_{\rm amp}$, MOS dividers are used to avoid resistive load. The final stage uses a resistor divider to implement a linear CMFB. The nominal quiescent current of the output stage can be simply set by the output common-mode voltages of the second stage. The second-stage amplifiers $P_{\rm amp}$ and $N_{\rm amp}$ are configured by a differential pair with diode-connected transistors as loads. The gain of each stage is determined by the g_m ratio of the differential pair and the load. A CMFB is required in $N_{\rm amp}$ to control the gain separately from the output stage quiescent current. In these stages, the random offset voltages caused by device mismatch have minor influence to the quiescent current because of the low gain. The worst-case offset derived from the device sizes in $P_{\rm amp}$ and $N_{\rm amp}$ will vary the quiescent current by only ± 200 μA. The simulated static linearity for a full-scale signal with presence of this offset is better than 120 dB. The small g_m variation in the output stage makes zero nulling resistors effective in the nested Miller compensation [16]. The simulated opamp dc gain is 110 dB. The gain bandwidth with a 50-pF load is 40 MHz. The static power supply current is 25 mA. The relaxed bandwidth requirement of direct charge transfer allows use of pMOS transistors for the input differential pair to reduce $1/f$ noise, which contribution is -123 dB relative to a full-scale sinewave. Since the opamp is in a follower configuration during $\phi 2$, and the bandwidth is limited by the output parasitic capacitance, wideband thermal noise of the amplifier does not alias and has negligible influence.

B. Reference Voltage Concerns

Another important issue in the analog design is the voltage reference. A reference voltage with analog noise substantially lower than the 120-dB target would require an unacceptable amount of power. In this design, the power supply is used as the voltage reference, which has no analog random noise and requires no extra power. Using this scheme, the power-supply rejection ratio of the DAC becomes 0 dB. A dedicated power pin for the reference voltage with an external bypass capacitor makes this approach feasible in this application. Although the impedance is lowered by the bypass capacitor, signal dependent modulation on the reference may cause severe distortion [17]. For example, linear signal dependency on the reference results in second-order harmonic distortion. The DCT scheme helps reduce this signal dependency. In the SC DAC, the reference provides only the charge difference between the new input and the previous output. As a result, the signal dependency of the reference load is suppressed by first-order noise shaping. The suppression for a 1-kHz signal is approximately 50 dB.

IV. Chip Implementation

Fig. 11 shows the block diagram of the complete stereo DAC for DVD-audio. An IIR filter with a pole at 3.2 kHz and zero at 10.6 kHz implements the 50/15 μs response de-emphasis function prior to the interpolator. The interpolation is performed in four stages. The first two stages are implemented

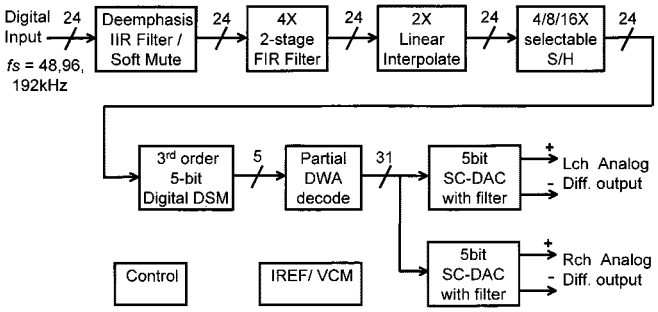

Fig. 11. Audio DAC block diagram.

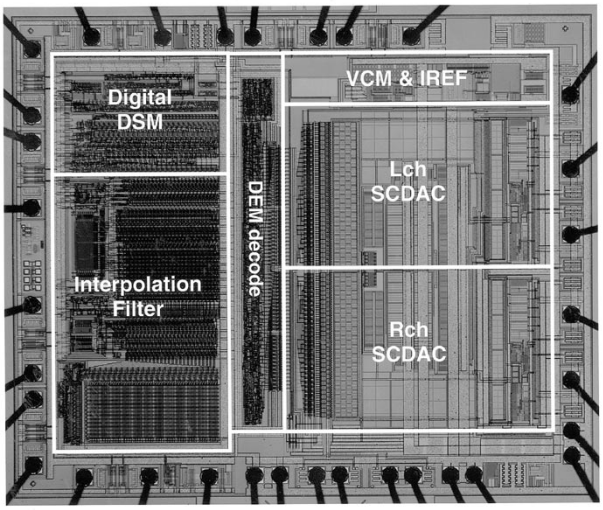

Fig. 12. Chip micrograph.

using half-band FIR filters to take advantage of the zero value coefficients and simplify the multiply–add process. The first and second-stage FIR filters are 95-tap and 15-tap, respectively. The third stage is 3-tap linear interpolation filter, while the last stage is a simple sample/hold register. The interpolation filter has a pass-band ripple of 0.005 dB and stop-band attenuation of 75 dB. A selectable interpolation ratio of 16×, 8×, or 4× allows a fixed oversampling frequency in the $\Delta\Sigma$M for all three input-sampling rates with a small circuit overhead. A fixed oversampling frequency reduces the design complexity in the analog circuit. The entire digital data-path including digital filtering, $\Delta\Sigma$M, and the DEM processing is time-shared by the left and right channels to reduce circuit area. The analog circuits of the two channels are separate and individual.

The chip micrograph of the audio DAC is shown in Fig. 12. The chip measures 3.1×2.5 mm^2 in 0.5-μm double-poly triple-metal (DPTM) CMOS, and is packaged in a 28-pin VSOP. The active area is 45% digital and 55% analog. The DEM overhead is 6% of the total die area. In the digital, a custom data-path layout reduces digital switching noise.

V. Measured Results

All measurements were taken by a commercial audio analyzer[2] in the balanced configuration with a second-order Sallen–Key filter on each side of the differential DAC output

[2]Rhode and Schwarz, *Operating Manual: UPD Audio Analyzer*.

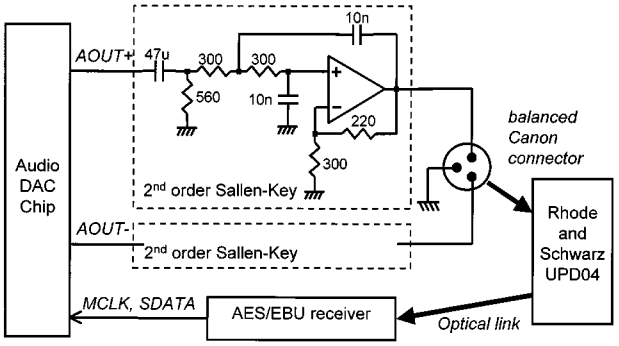

Fig. 13. Measurement setup.

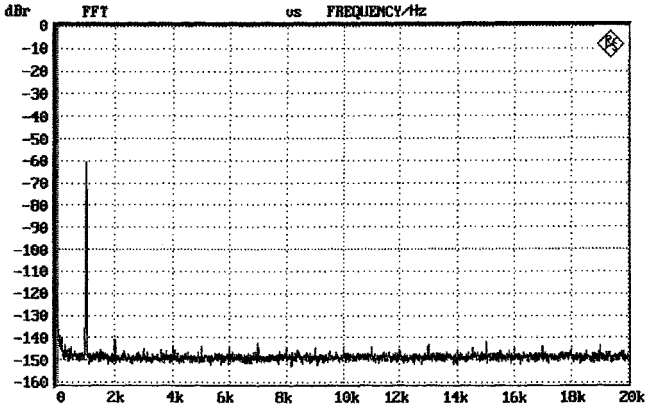

Fig. 14. 8192-point FFT at 1 kHz −60 dBr.

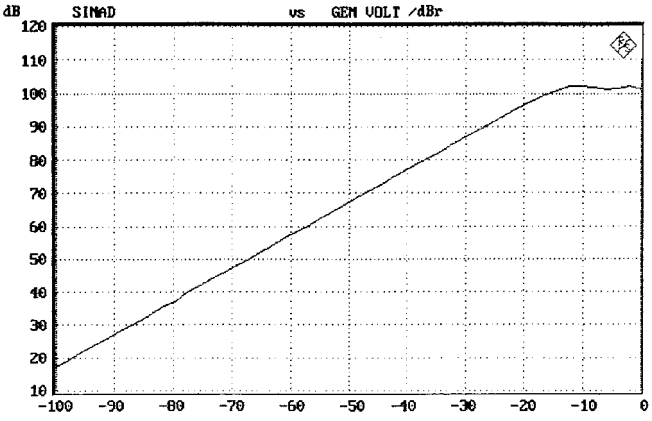

Fig. 15. SNDR versus input level at 1 kHz.

(Fig. 13). An industry standard AES/EBU receiver IC was used for the serial audio data interface and clock generation. An optical data link between the test board and audio analyzer was used for better isolation. Fig. 14 shows an 8192-point fast Fourier transform (FFT) spectrum of a 1-kHz −60 dBr signal at $f_s = 48$ kHz. The noise floor is approximately −150 dBr, and the largest spurious inband tone is smaller than −140 dBr. Fig. 15 shows the SNDR versus input level from −100 dBr to full-scale for a 1-kHz signal. The measurement bandwidth is 20 kHz. For audio applications, dynamic range is usually calculated as SNDR at −60 dBr, which is 57 dB. This yields 117-dB dynamic range. With A-weighting, the dynamic range becomes 120 dB. The SNDR at full-scale is 102 dB. An FFT spectrum for a full-scale signal is shown in Fig. 16. A 40-dB

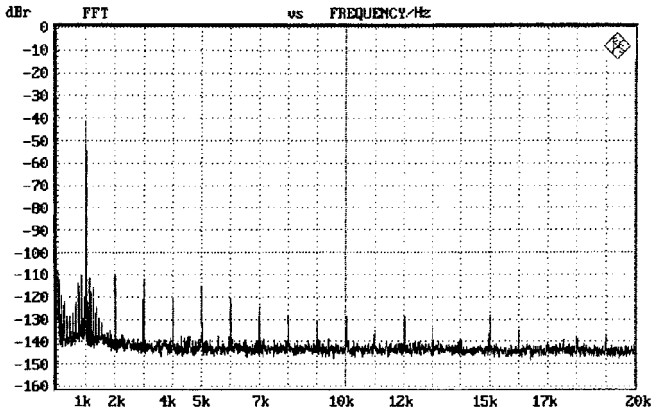

Fig. 16. 8192-point FFT at 1 kHz 0 dBr (−40-dB notch at fundamental).

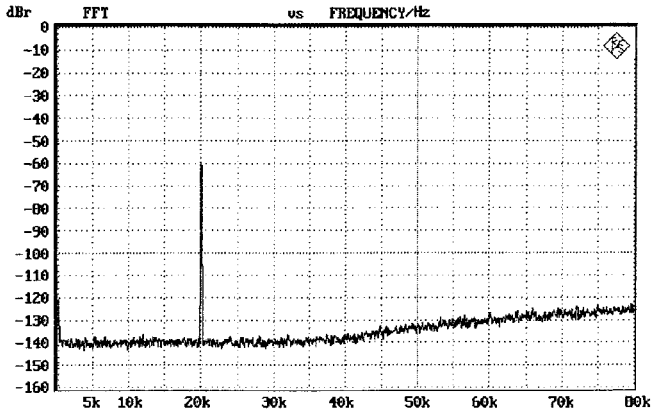

Fig. 17. FFT at 192-kHz sampling rate of a 20-kHz −60-dBr signal.

TABLE I
DAC PERFORMANCE SUMMARY

Specification	Performance	Comments
Output swing	±2.5Vpp	differential
Dynamic range		@ -60dBr,1kHz
fs=48kHz	120dB	20kHz BW, A-weight
fs=96kHz	113dB	40kHz BW
fs=192kHz	103dB	80kHz BW
Full power SNDR		@ 0dBr, 1kHz
fs=48kHz	102dB	20kHz BW
fs=96kHz	96dB	40kHz BW
fs=192kHz	93dB	80kHz BW
Channel Separation	120dB	@ 0dBr, 1kHz
Power dissipation	310mW	290mW(analog)
Chip size	7.8mm^2	0.5um DPTM

notch at the 1-kHz fundamental is placed after the DAC to lower the noise floor of the audio analyzer. At large signal level, the effect of clock jitter modulating the signal itself becomes more significant than the modulation of high-frequency quantization noise. The spurs at the side bands of the fundamental frequency indicate this effect. The third harmonic distortion is mainly caused by the second-order voltage dependency of the sampling capacitors [18]. The even-order harmonics are a result of intermodulation between the fundamental and third harmonic caused by digital noise coupling. Fig. 17 shows an FFT spectrum of a 20-kHz −60-dBr signal at $f_s = 192$ kHz. The rise of the noise floor above 40 kHz is caused by the $\Delta\Sigma$M quantization noise. The DAC performance is summarized in Table I. The dynamic range at sample rates of $f_s = 96$ kHz and 192 kHz are 113 dB and 103 dB, respectively. Channel separation between the two audio channels is more than 120 dB. The total power dissipation is 310 mW.

VI. CONCLUSION

In conclusion, several design techniques useful for realization of a high-end consumer audio DAC have been presented. A 5-b $\Delta\Sigma$ DAC architecture optimized for jitter tolerance allows use of commercially available audio interface IC's, while achieving the high-end performance. Partial DWA takes advantage of the high-end audio application requirements like large capacitor sizes and gaussian distribution of audio signals to make mismatch-induced noise power negligible with reduced circuit overhead compared to conventional DWA. The SC DAC with hybrid filter implements the 5-b DAC function and post filtering required for jitter tolerance using a single opamp. Also, unlike a conventional SC implementation, use of the DCT scheme makes power dissipation limited by output drive requirements instead of kT/C noise constraints. A 24-b 5-V stereo audio DAC for DVD-audio playback has been developed using these techniques. The DAC achieves 120-dB A-weighted dynamic range, which exceeds the previously reported high-end consumer audio DAC by 4 dB [2].

REFERENCES

[1] T. Soh, "Five semiconductor makers to ship 24-bit DAC LSI's for use in audio equipment" (in Japanese), *Nikkei Electron.*, no. 706, pp. 51–56, Jan. 1998.
[2] R. Adams, K. Nguyen, and K. Sweetland, "A 116 dB SNR multibit noise-shaping DAC with 192 kHz sample rate," presented at the 106th AES Convention, Preprint 4963, May 1999.
[3] I. Fujimori, A. Nogi, and T. Sugimoto, "A multibit delta–sigma audio DAC with 120 dB dynamic range," in *ISSCC Dig. Tech. Papers*, Feb. 1999, pp. 152–153.
[4] I. Fujimori and T. Sugimoto, "A 1.5 V, 4.1 mW dual-channel audio delta–sigma D/A converter," *IEEE J. Solid-State Circuits*, vol. 33, pp. 1879–1886, Dec. 1998.
[5] S. Norsworthy, R. Schreier, and G. Temes, *Delta–Sigma Data Converters: Theory, Design, and Simulations*. New York, NY: IEEE Press, 1996.
[6] D. Knapp *et al.*, "A family of AES/EBU interface devices," presented at the 89th AES Convention, Preprint 2962, Sept. 1990.
[7] R. Baird and T. Fiez, "Linearity enhancement of multibit delta–sigma A/D and D/A converters using data weighted averaging," *IEEE Trans. Circuits Syst. II*, vol. 42, pp. 753–762, Dec. 1995.
[8] K. Hamashita and E. Swanson, "A single chip stereo audio CODEC," in *Proc. 1993 IEEE CICC*, May 1993, pp. 28.4.1–28.4.4.
[9] L. Williams, "An audio DAC with 90 dB linearity using MOS to metal-metal charge transfer," in *ISSCC Dig. Tech. Papers*, Feb. 1998, pp. 58–59.
[10] A. Yasuda, H. Tanimoto, and T. Iida, "A third-order $\Delta\Sigma$ modulator using second-order noise-shaping dynamic element matching," *IEEE J. Solid-State Circuits*, vol. 33, pp. 1879–1886, Dec. 1998.
[11] R. Adams, K. Nguyen, and K. Sweetland, "A 113 dB SNR oversampling DAC with segmented noise-shaped scrambling," *IEEE J. Solid-State Circuits*, vol. 33, pp. 1871–1878, Dec. 1998.
[12] N. S. Sooch, J. W. Scott, T. Tanaka, T. Sugimoto, and C. Kubomura, "18-b stereo D/A converter with integrated digital and analog filters," presented at the 91st AES Convention, Oct. 1991.
[13] D. Haigh and B. Singh, "A switching scheme for switch capacitor filters which reduces the effect of parasitic capacitances associated with switch control terminals," in *Proc. 1983 IEEE ISCAS*, May 1983, pp. 586–589.
[14] D. Su, "Oversampling Digital-to-Analog Conversion," Ph.D. dissertation, Stanford Univ., Aug. 1994.

[15] H. Khorramabadi, "A CMOS line driver with 80-dB linearity for ISDN applications," *IEEE J. Solid State Circuits*, vol. 27, pp. 539–544, Apr. 1992.
[16] R. G. H. Eschauzier and J. H. Huijsing, *Frequency Compensation Techniques for Low-Power Operational Amplifiers*. Norwood, MA: Kluwer, 1995.
[17] S. Harris, "How to achieve optimum performance from delta–sigma A/D and D/A converters," *J. Audio Eng. Soc.*, vol. 41, pp. 782–790, Oct. 1993.
[18] G. Yin and W. Sansen, "A high-frequency and high-resolution fourth-order $\Delta\Sigma$ A/D converter in BiCMOS technology," *IEEE J. Solid-State Circuits*, vol. 29, pp. 857–865, Aug. 1994.

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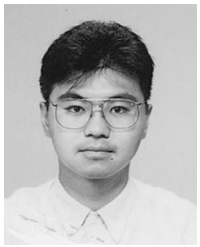

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