Continuous-Time Sigma-Delta Modulator with an embedded Pulse Width Modulation

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Abstract— **A new continuous-time Sigma-Delta (SD) modulator, called a Pulse-Width (PW)-SD modulator is proposed where the flash quantizer of a conventional multibit modulator is replaced by a comparator with hysteresis and one sampler clocked at a higher rate, providing a PW modulated digital output. As the proposed modulator only requires a single-bit DAC, less power consumption and silicon area are expected when compared to a conventional multibit modulator with the same performances. Furthermore, unlike the conventional single-bit modulator, when the Dynamic Range in the proposed modulator is increased by increasing the sampling rate, the integrators maintain their unity-gain frequencies, keeping the same power consumption and area occupancy. The proposed modulator is not an asynchronous SD modulator, as the output signal is digital and the sampler is inside the loop. An approximate theoretical analysis of the proposed modulator is given which is validated by simulation in the time-domain. Finally, experimental results from a prototype board with commercial components show that this implementation is feasible, although some drawbacks, as distortion level, could be avoided in an integrated realisation.**

Index Terms— **Continuous Time Sigma Delta Modulation, Pulse-Width Sigma-Delta Modulation, Asynchronous Sigma-Delta Modulation.**

I. Introduction

SIGMA-Delta (SD) modulation has been extensively applied to data conversion [1]. The signal to be converted is sampled and digitized using a quantizer embedded in a high-gain loop. Despite the low resolution of the quantizer, the overall modulator can achieve a high resolution due to oversampling and noise shaping. Other well-known modulation schemes, such as Pulse Width (PW) modulation, have been used for power converters [2] and class-D amplifiers. In an ideal PW modulator, a DC input value X is converted to an output pulse stream with mean value X. Sinusoidal and other time-varying waves can also modulate the pulse width of the carrier signal. If the carrier frequency is much greater than the maximum frequency of the input signal, this can be reconstructed from the modulated output signal by low-pass filtering, obtaining a high Signal-to-(Noise+Distorsion) ratio (*SNDR*).

Figure 1 (with t_S =0 and no Digital-to-Analog Converter (DAC)) shows the well-known asynchronous sigma-delta modulator [3]-[4], where the quantizer embedded in a SD loop has been replaced by a comparator with hysteresis. If $x(t)=X$ is a DC value, the integrator output is a triangular signal with a rising slope of $w_2\cdot(X+V_S)$ and a falling slope of $w_2\cdot(X-V_S)$. The rectangular signal $y(t)$ takes the value $+V_S$ during a time interval T_p and the value $-V_S$ during a time interval T_n, with

$$T_p = \frac{\Delta}{w_2\cdot(V_S - X)} \quad \text{and} \quad T_n = \frac{\Delta}{w_2\cdot(V_S + X)} \tag{1}$$

where Δ is the hysteresis width. The frequency at the comparator output is

$$f(X) = \frac{1}{T_p + T_n} = \frac{w_2}{2}\cdot\frac{{V_S}^2 - X^2}{\Delta\cdot V_S} \tag{2}$$

whose maximum value is given by

$$f_{\max} = f(0) = \frac{1}{T_{\min}} = \frac{w_2\cdot V_S}{2\cdot\Delta} \tag{3}$$

The mean value of $y(t)$,

$$\bar{y} = V_S\,\frac{T_p - T_n}{T_p + T_n} \tag{4}$$

and it is exactly equal to X. Note that, in the architecture of Figure 1 (with t_S =0 and no DAC), the output signal is not quantized, that is, its DC value X can be extracted from $y(t)$ with an unlimited resolution using an ideal low-pass filter. If the input signal $x(t)$ is a slowly varying signal, it can be reconstructed from $y(t)$ with a high precision. In fact, $y(t)$ will be only corrupted by some harmonic distortion, but there will not be another error sources due to the lack of quantization noise. In a conventional PW modulator the frequency of the rectangular output signal is kept constant and the information is contained in the duty cycle, while in the modulator of Figure 1 (with t_S =0 and no DAC) the information is contained in both, the frequency and the duty cycle. Both modulators have similar performances when the carrier frequency of the conventional PW modulator is f_{max}. However, due to the lack of sampling, neither of them can be used for data conversion. Existing approaches to data conversion use a sampler located outside the loop [4], but the errors in the sampling process are not noise-shaped.

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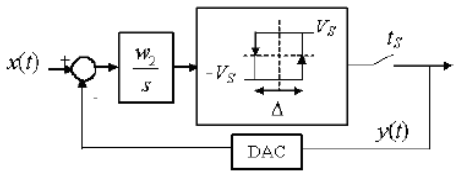

Figure 1: Proposed first-order PW-SD modulator including a comparator with hysteresis

II. THE FIRST ORDER PROPOSED MODULATOR

For the purpose of applying the architecture of Figure 1 to data conversion, a sampler and a single-bit DAC operating at a rate $f_S=1/t_S$ are placed following the comparator. Due to sampling, the new values of T_p and T_n are represented as $T_p= k\cdot t_S$ and $T_n= l\cdot t_S$, where k and l are integer numbers. When compared to the asynchronous modulator presented above, the main difference is that, now, the input value X can be extracted from the modulated signal y(t) with only a finite precision. The minimum resolution of y(t) is determined by the area contained in a rectangular pulse of height $\pm V_S$ and width t_S (Figure 2). Assuming that $f_S >> f_{max}$, and for a small DC input signal X, the period of y(t) is approximately equal to T_{min} (Eq. (3)), so that $T_p+ T_n = (k + l) \cdot t_S \approx T_{min}$. The output y(t) is fed back to the modulator input and its mean value is obtained by integration at successive time periods of approximately T_{min} seconds. In this way, quantization in the time domain at the modulator output is converted to quantization in amplitude at the integrator output. The amplitude resolution is given by

$$q = V_S \cdot t_S \cdot w_2 = V_S \cdot w_2 / f_s \qquad (5)$$

As a conclusion, the architecture depicted in Figure 1 can be considered to be equivalent to a first-order SD modulator with a multibit quantizer of step $q = V_S \cdot w_2 / f_S$, sampled at a rate $f_{max}=1/T_{min}$. Therefore, the effective number of bits of the quantizer is $m = \log_2 (2\cdot V_S / q) = \log_2 (2\cdot f_S / w_2)$.

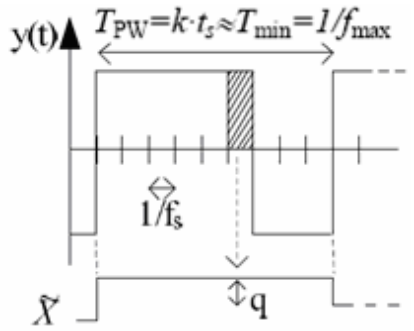

Figure 2: Sampled output signal y(t) and demodulated signal $\widetilde{X}$

Although this result is only valid for slowly varying input signals, this assumption is normally accepted for oversampled converters. Furthermore, these conclusions can be extended to high-order modulators, as it will be shown next.

III. THE SECOND ORDER PROPOSED MODULATOR

Figure 3.a shows the second-order version of the proposed PW-SD modulator. Assuming again that the input signal is a DC value X and no sampling (i.e., t_S=0 and no DAC), the modulator output y(t) is a rectangular wave which takes a value V_S during T_p seconds, and a value $-V_S$ during the rest of the period (T_n seconds). Therefore, the first integrator output v_1(t) is, once again, a triangular wave of period T_p+T_n.

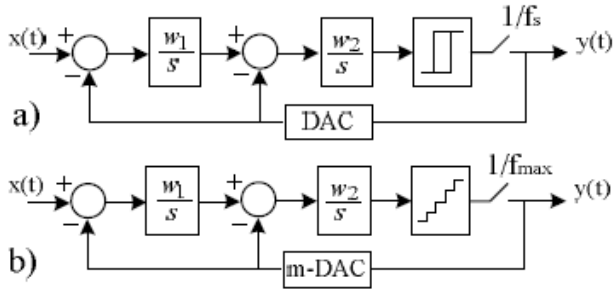

Figure 3: a) Proposed second-order PW-SD modulator and b) Conventional multibit SD with $q = V_S \cdot w_2 / f_S$

The second integrator output can be calculated from

$$v_2(t) = \frac{\Delta}{2} + w_2 \int_{t_0}^{t} [v_1(\tau) - y(\tau)] d\tau \quad , \quad t_0 \le t \le t_0 + T_p = t_1 \qquad (6)$$

$$v_2(t) = -\frac{\Delta}{2} + w_2 \int_{t_1}^{t} [v_1(\tau) - y(\tau)] d\tau \quad , t_1 \le t \le t_1 + T_n = t_0 + T_p + T_n \qquad (7)$$

In equations (6) and (7), t_0 and t_1 are the time instants where the comparator output changes. Assuming these conditions, the analysis of the architecture for the case t_S=0 and no DAC is straightforward. It can be shown that the equations (1)-(4) are still valid. The output swing of the first integrator is between the limits

$$v_1(t_1) = X - \frac{\Delta}{2} \cdot \frac{w_1}{w_2} \quad \text{and} \quad v_1(t_0) = X + \frac{\Delta}{2} \cdot \frac{w_1}{w_2} \qquad (8)$$

and the output swing of the second integrator is limited by $\pm\Delta/2$.

In the case of sampling (t_S >0 and a single-bit DAC), following the same reasoning as in the first-order case, the performances of the proposed modulator in Figure 3.a are expected to be equivalent to those of a conventional one shown in Figure 3.b, which is clocked at the rate f_{max} (Eq. (3)), with a quantization step q given in Eq. (5). Note that for the equivalent multibit of Figure 3.b, with a sinusoidal wave of amplitude A and a noise bandwidth $f_b = f_{max}/(2\cdot OSR)$, (where OSR is the Oversampling Ratio), the Signal-to-Noise Ratio (SNR) obtained from a linear analysis (SNR_{pr}) is given by [1]:

$$SNR_{pr} = \frac{60}{\pi^4} \cdot C \cdot \frac{A^2}{2}\left(\frac{1}{q}\right)^2 \cdot OSR^5 \qquad (9)$$

with the modulator coefficients $C = \frac{{w_1}^2 \cdot {w_2}^2}{{f_{max}}^4}$, step quantization given by equation (5) and oversampling ratio given by $OSR = \frac{f_{max}}{2 \cdot f_b}$

Comparing the performances of the proposed modulator with those of the conventional multibit, for the same noise bandwidth f_b, the *SNR* of a conventional single-bit modulator (SNR_{co}), where $q_{conv} = 2 \cdot V_S$, with integrator gains ($\alpha \cdot w_1$, $\alpha \cdot w_2$), clocked at a rate $\alpha \cdot f_{max}$ is given by:

$$SNR_{co} = \frac{60}{\pi^4} \cdot C_{conv} \cdot \frac{A^2}{2}\left(\frac{1}{q}\right)^2 \cdot {OSR_{conv}}^5 \qquad (10)$$

with $C_{conv} = \frac{(\alpha \cdot w_1)^2 (\alpha \cdot w_2)^2}{\alpha \cdot {f_{\max}}^4}$, $\frac{1}{q_{conv}} = \frac{1}{2 \cdot V_S}$ and $OSR_{conv} = \frac{\alpha \cdot f_{\max}}{2 \cdot f_b}$

Expressions (9) and (10) are equal when the factor is $\alpha = (2 \cdot f_S / w_2)^{2/5}$. That is, the conventional single-bit SD modulator can achieve the same *SNR* than the *SNR* of the proposed one when it is clocked at a rate α times greater than f_{max}. Note that the integrator gains of the former modulator compared with those of the proposed one have to be increased by the same factor.

IV. Results from Simulations

A. SNR of the PW-SD modulator

The architecture shown in Figure 3 was simulated using different values of w_1, w_2, Δ, V_S, and f_S. Figure 4 shows the *SNDR* curves for w_1=w_2= 704 KHz, V_S =1 V, and Δ=1/2. The sampling rate of the equivalent multibit SD modulator is given from Eq. (3), f_{max}=704 KHz. The oversampling ratio is chosen to be *OSR*=16 leading to a noise bandwidth of f_b=22 KHz. The proposed modulator has been simulated in the time domain with a sinusoidal input signal of 4.3 KHz and different values of $F = f_S / f_{max}$. The *SNR* obtained from Eq. (9) matches the simulated *SNDR* for the proposed modulator with values of *F* greater or equal than 4 as shown in Figure 4. Note that the *SNDR* of the proposed architecture increases by, approximately, 6 dB when the frequency of the sampler is doubled, but the integrators do not require a higher speed (that is, the integrator constants w_1 and w_2 have the same value in all the simulations).

Furthermore, according to Eq. (10), to obtain the same *SNR*, the speed of a conventional single-bit modulator should be increased by a factor $\alpha=(2f_S/w_2)^{2/5}$. In our example, for f_S/w_2=8, α=3.03. This result has been verified by simulation.

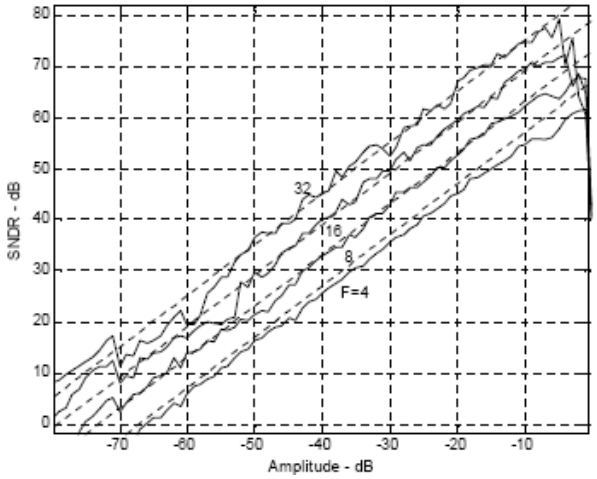

Figure 4: *SNR* given by expression (9) (dashed line), and simulated *SNDR* of the proposed modulator (solid line) for different values of $F=f_S/f_{max}$.

B. Spectrum of the modulator output

For the set of parameters given above the Power Spectrum Density of the output signal is depicted in Figure 5. The upper figure represents the spectrum for the case t_S =0 and no DAC. As discussed in section 1, the asynchronous modulator is an analog modulator whose output is only corrupted by harmonic distortion. Assuming the case of t_S >0 and a single-bit DAC, the PSD is depicted in the lower figure. Now the quantization noise produced by the finite time resolution of the PW-SD modulation can be observed and the modulator is free from harmonic distortion due to the dithering effect introduced by this noise.

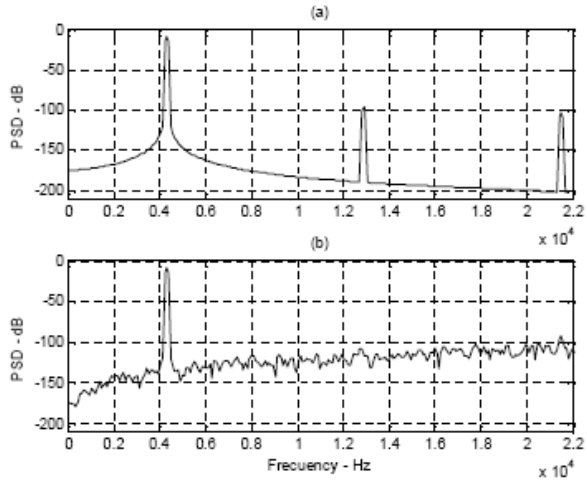

Figure 5: Power Spectrum Density of the modulator output in the signal band for (a) asynchronous modulator (ts=0 and no DAC), and (b) proposed modulator (ts>0 and a single-bit DAC) with F=8

V. Gain Bandwidth Product and Slew Rate in the OpAmp at the First Integrator

One of the most contributors to limitations for overall modulator DR is the first integrator [5]-[6]. In order to determine the Gain-Bandwidth (*GBW*) limitations of the OpAmp in the first integrator, this effect has been modelled using Simulink®.

A common practice to guarantee stability is to design the OpAmp with a dominant pole, so that its frequency response can be treated as a first–order transfer function. Figure 6 shows the *SNDR* degradation produced in the performances of the overall PW-SD (labelled "hyst") and equivalent multibit (labelled "conv") modulators. As it can be seen, the degradation is comparable in both modulators.

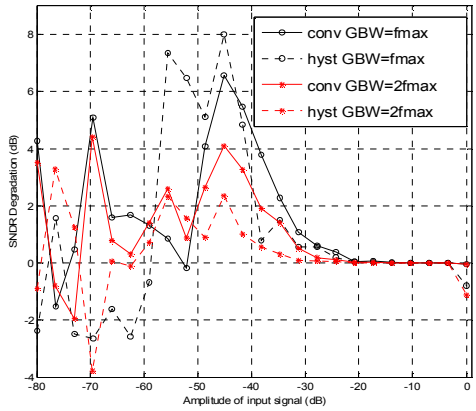

Figure 6: Degradation of *SNDR* due to *GBW* of the OpAmp at the first integrator for the conventional multibit SD and the equivalent proposed PW SD

Despite the sampling rate in the PW-SD modulator is *fs*, the frequency requirements of the amplifiers are limited as in the case of a modulator rated at f_{max}. Finally, for the parameter values given in Section IV and input amplitude of 0.8 V, it is necessary a minimum slew rate of 1.5V/μs to avoid slewing problems in the amplifiers.

VI. Non Idealities Effects of PW-SD Modulator

A. Excess Loop delay

The excess loop delay (ELD) may result in *SNR* performance degradation or even instability. The proposed modulator has shown to be robust against this problem, with only 4dB *SNDR* degradation (for factor F=8) in the worst case, for an excess loop delay in the interval [0, T_S], while the conventional multibit SD modulator turned out to be unstable in that interval.

B. Jitter Noise

Figure 7 shows the degradation in *SNDR* due to jitter noise produced for different values of the standard deviation $\sigma_{\Delta t}$ (labelled "sigma") of the Gaussian noise for the conventional single bit (labelled "sb") and the proposed (labelled "hyst") modulators. The sampling rate and the *GBW* of the integrators in the former modulator have been increased in order to get the same performances than those of the proposed one. As it can be seen, the robustness against jitter is comparable in both modulators.

C. Pulse Shape of DAC

To test the robustness of the proposed modulator, the transitions at the DAC output have been modelled as an

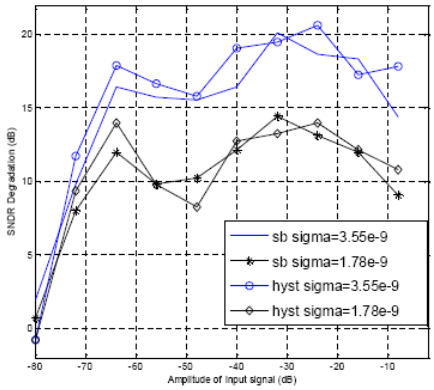

Figure 7: Degradation of *SNDR* due to jitter noise in DAC for different values of standard deviation

exponential wave with a time-constant τ. The *SNDR* curves for the conventional multibit modulator (Figure 3.b) clocked at the rate f_{max} and that of the proposed one (Figure 3.a) are presented in Figure 8 for an input signal amplitude of –10 dB, F=8, different values for τ, and different values for the relative mismatch between the rising and falling time constants. This figure shows that the sensitivity of the proposed modulator to the DAC pulse is better than that of the equivalent multibit modulator. This effect is especially significant for low values of F. Furthermore, different simulations have been carried out comparing the proposed modulator with different values of F to a single-bit conventional one with large *OSR*'s so that they have the same Dynamic Range. The proposed modulator is nearly insensitive to the mismatch between the time constants of the rising and falling edges of the DAC pulse while the Dynamic Range of the conventional single-bit DAC drops for about 17 dB for a modest 1% mismatch (this value corresponds to the case F = 8, $1/(2\,\tau\,f_{max})$ = 16).

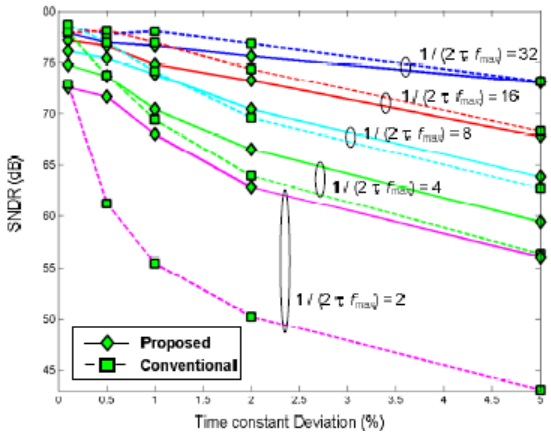

Figure 8: *SNDR* degradation caused by mismatch between the rising and falling time constants of the DAC output for the proposed and the conventional modulators

From the design point of view, even though the comparator in the proposed modulator is clocked at the rate f_S, the specifications of the DAC are equivalents to those of a DAC clocked at the rate f_{max}.

VII. Simulation Results from SPICE

The electronic schematic of the second order modulator, implemented with commercial devices in a prototype board, is depicted in Figure 9. Both integrators are implemented

using RC-OpAmps scheme. For them, two different OpAmps are tested, LM741 and OP-37. The comparator with hysteresis is implemented using OpAmp LF357. The switches in the DACs are implemented using MOSFET BS170.

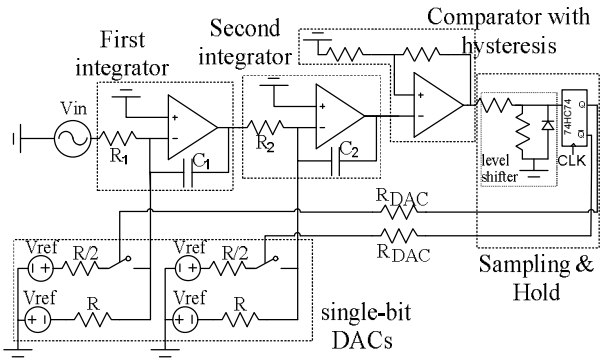

Figure 9: Schematic circuit implemented in the prototype board

Considering the pessimistic condition that both inputs to the integrators (signal and feedback paths) take the maximum voltage level, the variation speed at the integrator outputs is given by $2 \cdot V_S \cdot w_i$, i=1 or 2, where V_S, w_1, and w_2 are given in Table I, for this prototype board. If the Slew Rate (SR) of the amplifiers in the first and second integrator is greater than 256 KV/s and 512 KV/s, respectively, the integrators will not operated in slewing regime. As the slow OpAmp LM741 has a SR of 500 KV/s, the linear operation of the integrators is guaranteed.

TABLE I
VALUES OF THE PARAMETERS IN THE SIMULATED MODULATOR AND IN THE EQUIVALENT MULTIBIT MODULATOR

Proposed Modulator		Equivalent Multibit Modulator	
Parameter	Value	Parameter	Value
Signal Bandwidth	300 Hz	Signal Bandwidth	300 Hz
Sampling rate (f_s)	128 KHz	Sampling rate (f_{max})	28.4 KHz
w_1	32 Krad/s	w_1	32 Krad/s
w_2	64 Krad/s	w_2	64 Krad/s
Δ	4.5 V	Quantization step (q)	2 V
V_S	4 V	Levels in quantizer	5 levels

In order to detect the most critical component of the circuit, simulations have been launched using ideal components and models provided by the manufacturer of the components. Table II summarizes the results obtained from SPICE for a sinusoidal input of 600 mV (-16.5 dBFS) and 63 Hz.

TABLE II
SNR AND SDNR VALUE FOR DIFFERENT TESTS WITH SPICE FOR A SINUSOIDAL INPUT OF 600 MV (-16.5 DBFS) AND 63 HZ.

Test	Configuration	SNR(dB)	SNDR(dB)
A	MATLAB/SIMULINK	74.520761	74.520761
B	Complete ideal	72.773671	72.773671
C	OpAmp-LM741	71.277732	69.346179
D	Comparator-LF357	68.403834	60.483834
E	Switch-BS170	61.888859	59.643497

Row labelled "A" corresponds to the results obtained from Matlab/Simulink® for the second order proposed modulator. Row B is obtained from SPICE using ideal models to simulate all the components (dependent voltage sources with large value of gain for the OpAmps in the integrators and comparator, and ideal switches for the DAC). In order to detect the component that produces more degradation in the modulator performances as compared to the ideal case in test B, from tests C to E, one of the ideal models is replaced by the SPICE model provided by the manufacturer. For instance, in Test C the OpAmps in the integrators are LM741, the OpAmp in the comparator and the switches in the DAC are ideal. In test D only the ideal OpAmp in the comparator is replaced by LF357. In test E the influence of the switches is studied replacing these components by the MOSFET transistor BS170.
According to Table II, nearly 12.5 dB is expected to be lost in an electronic implementation as compared to the ideal case of Tests A or B. The most critical component is the transistor BS170. An alternative implementation of the switches could be achieved using the bipolar transistor 2N2222A. Nevertheless, simulations reveal that the rise and fall times are comparable to the sampling period t_S. The distortion is reduced using the bipolar transistor but a considerable degradation in the *SNR* is produced due to an increase of the noise floor.

Note that, in an integrated implementation using CMOS technologies, the gate size of the MOS transistor can be minimized in order to reduce the charge injection and the clock feedthrough. In this way, the performance degradation in the *SNDR* produced by the transistor BS170 is overcome in an integrated implementation.

VIII. EXPERIMENTAL RESULTS

As it can be seen from section above, this modulator could reach approximately 12 bits of resolution using the well-known OpAmp LM741. Measurements have been obtained using a sinusoidal input signal generated by an accurate signal generator from AudioPrecision®. The bitstream output is captured with a logic analyser and then, the data are post-processed with Matlab®.
As in the case of SPICE simulations, several commercial devices have been utilized in the prototype board in order to study any limitation of speed and linearity imposed by the real components. In Table III, *SNDR* and *SNR* values for different tests are described when it is applied a sinusoidal input of 600 mV (-16.5 dBFS) and 63 Hz.

TABLE III
EXPERIMENTAL VALUES OF SNR AND SNDR VALUES FOR DIFFERENT TESTS WITH PROTOTYPE BOARD FOR SINUSOIDAL INPUT OF 600 MV (-16.5 DBFS) AND 63 HZ

Test	Configuration	SNR (dB)	SNDR (dB)
F	LM741 and BS170	57.889326	50.529337
G	OP37 and BS170	58.543421	51.623457
H	OP37 and 2N2222	54.416250	49.286742

In Test F, the OpAmps are LM741 and the switches are MOS BS170. In Test G, OpAmps OP37 are used for the integrators in order to determine the influence of the *GBW*. Finally, the influence of switch commutation is studied in test H, where the fast OpAmps and bipolar switches are used.

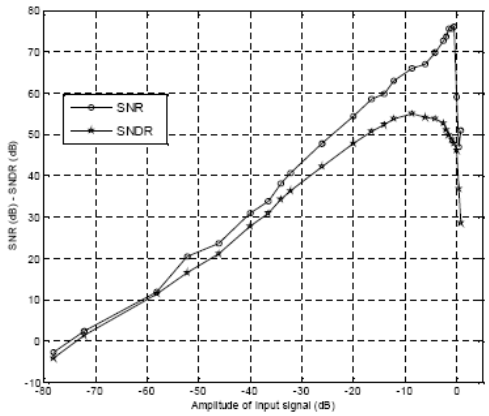

Figure 10: Experimental values of *SNR* and *SNDR* for prototype board. The signal frequency is 63 Hz and the sampling frequency of 128 kHz.

Using the same components as in Test F, Figure 10 shows the experimental values of *SNR* and *SNDR* measured for different input amplitudes. As it can be seen from this, a lost of *SNDR* in comparison with *SNR* is observed. The results for different values of f_S are shown in Figure 11 where the prototype board achieves 74.8 dB (12.13 bits) for sampling frequency of 128 kHz and 82.4 dB (13.40 bits) for sampling frequency of 256 kHz, with 300 Hz of signal bandwidth.

From Tests B, E, F, and output spectrum, it is shown that the first distortion source in the prototype is the MOS transistor used as switch. Despite the transistor BS170 is not a power device, it supports high currents (500mA) and has very large parasitic capacitances in comparison with the capacitances of an integrated device. In an integrated realisation, the switches can be implemented using transistor with gate dimensions as smaller as technology allows, in order to reduce the charge injection and the clock feedthrough [7]. Note that the distortion in Figure 10 is due to even order harmonics. The even order distortion could be reduced or even rejected in a complete differential scheme, commonly used in integrated implementations. In conclusion, the distortion problem can be avoided in an integrated solution.

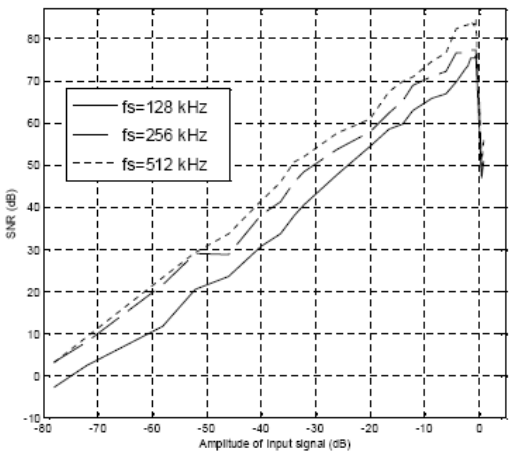

Figure 11: Experimental values of *SNR* versus amplitude of input signal, for sampling frequency of 128 kHz, 256 kHz and 512 kHz

IX. CONCLUSIONS

A novel Sigma Delta modulator with PW modulation has been proposed. Several advantages of this new architecture in comparison with its equivalent multibit conventional SD are presented and confirmed by simulations and experimental results in a prototype board built with commercial components.

The multibit quantizer and the multibit DAC in the conventional SD modulator are replaced by a comparator with hysteresis and a single bit DAC rated at f_S in the proposed modulator, respectively. So, complexity is relaxed for this new structure at expense of higher sampling frequency. This new modulator is sampled at frequency f_S, while the conventional multibit SD is sampled at f_{max}. Nevertheless, in the proposed SD, the OpAmps in the integrators are dimensioned for the frequency f_{max}, although the circuit is sampling at f_S, where $f_S >> f_{max}$.

Gain bandwidth product and finite dc gain in first integrator and well-known non idealities effects, as excess loop delay and jitter noise, are studied in both architectures and the robustness of the proposed modulator is proved.

Simulation results with Matlab/Simulink® and SPICE are shown in order to demonstrate that conventional multibit Sigma Delta and the proposed PW SD are equivalent. Experimental results for prototype board show that this implementation is feasible, although some drawbacks, as distortion level, could be avoided in an integrated realisation. The simulations reveal that while the integrators (and amplifiers) keep their speed constraints, doubling f_S, the output *SNDR* is increased by 6 dB (1 equivalent bit). An analytical study has provided theoretical results which are in agreement with simulation results.

Finally, the proposed PW-SD is expected to consume less power and silicon area than the conventional multibit one due to the lack of multibit converters. The proposed modulator solves the problems of the asynchronous SD ones, by providing a digital output while keeping the quantization noise inside the SD loop.

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