A Multi-bit Switched Capacitor DAC with Robust Analog Background Calibration

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***Abstract*—A multi-bit switched-capacitor DAC with robust analog background calibration intended to be used as feedback DAC for multi-bit pipeline ADCs or broadband sigma delta ADCs with low oversampling ratio is presented in this paper. The accuracy of calibration is not limited by mismatch of charge injections. A multi-bit switched-capacitor DAC whose linearity is only limited by opamp DC gain is realized. Assuming mismatch in capacitor values, switch transistor threshold voltages and opamp offsets, simulation results show linearity improves by about 40dB to 15-bit after about 900 sampling clock periods.**

I. INTRODUCTION

Multi-bit feedback DACs are used in delta-sigma modulators or pipelined ADCs to reduce opamp output swing thus linearity requirement of the integrators [1] or inter-stage gain accuracy requirement in case of pipeline ADC [2]. Since CMOS process can only match capacitor up to 10~12 bit and the matching degrades for smaller capacitors, some kind of linearization of the multi-bit DAC is necessary if more than 10 bit resolution is desired for the entire ADC. When the oversampling ratio (OSR) is high, first order mismatch shaping techniques such as data-weighted averaging (DWA) are usually the best choice. However, when OSR is low or in case of pipelined ADC such as [3,4], first order mismatch shaping is no longer effective and much more complicated linearization techniques such as higher order mismatch shaping or digital noise cancellation (DNC) must be used. Such techniques require much design complexity and have potential stability problems (in the case of higher order mismatch shaping) or long convergence time (in the case of DNC).

Another solution is mismatch correction through analog calibration, which has a deterministic, usually much shorter convergence time. Although there exist many works on analog calibration techniques for the current-steering type DACs [5,6], little work has been done for switched-capacitor DACs which are necessary in most discrete-time data converters. Although continuous-time ΔΣ ADCs have seen increased application in communication products in recent years, the majority of data converters are still the discrete-time, switched-capacitor type. This is because switched-capacitor data converters are less sensitive to external environment such as clock jitter and digital noise. Their ease of use results in more customer acceptance. Reference [7] is the only published work to the authors' knowledge that proposes an analog calibration technique that can continuously correct for mismatch error in switched-capacitor DAC. The technique proposed in [7], however has two shortcomings: 1. the stability of the calibration loop is dependent on clock frequency, and 2. the achievable element matching is limited by switch charge injection mismatch.

In this paper, an improved technique is proposed that is fully implemented in discrete-time, switched-capacitor circuits. Therefore the circuit can work with any clock frequency, improving flexibility of the system. Furthermore, by an improved switching sequence, charge injection mismatch that limits the accuracy of many existing analog calibration techniques such as [5-7] has been eliminated. The DAC element matching becomes only limited by the calibration loop gain. The rest of this paper is organized as follows: section II provides an overview of the calibration structure, section III examines circuit non-idealities including charge injection, finite opamp gain and offsets, and section IV presents a design example and SPICE simulation results.

II. THE ANALOG CALIBRATION STRUCTURE

Fig. 1 illustrates an *N+1* level multi-bit switched capacitor DAC using the proposed calibration technique. The input to the DAC, D_{in}, is thermometer coded, therefore each DAC element should provide identical charge to the summing node of OTA1 for the DAC to be linear. *N+1* identical DAC elements are provided in the

proposed multi-bit DAC. One out of the *N+1* DAC elements is chosen at a time to be in calibration mode, while the other *N* DAC elements are connected to D_{in}, providing the *N+1* level signal to the summing node. A calibration capacitor C_{CAL} is connected in parallel with each DAC element capacitor, C_{DAC}, in a way such that each DAC element delivers the charge

$$Q_{DAC} = 2V_{REF}C_{DAC} - V_{OC}C_{CAL} \quad (1)$$

to the summing node of OTA1. Let's look at the DAC element in calibration mode. If there is mismatch between the reference C_{REF} and the C_{DAC} of the DAC element, the difference in charge will be integrated on capacitor C_{HOLD}, and the output of OTA_{CAL}, V_{OC}, will be adjusted until the error charge

$$Q_E \equiv Q_{DAC} - 2V_{REF}C_{REF} \quad (2)$$

settles to zero. When the calibration of this DAC element is finished, the virtual ground of OTA_{CAL} will stay disconnected and C_{HOLD} will continue to hold the voltage V_{oc} that satisfies $Q_E = 0$. The accuracy of C_{DAC} and C_{CAL} therefore is non-critical, since in steady state the charge delivered to the summing node will be equal to $2V_{REF}C_{REF}$. The maximum correctable range of error in C_{DAC} is given by

$$\Delta C_{DAC} \le \frac{C_{CAL}V_{swing}}{2V_{REF}}. \quad (3)$$

Assuming σ of 0.5% capacitor mismatch, C_{CAL} can be chosen using

$$C_{CAL} > 3\sigma C_{DAC} \times \frac{2V_{REF}}{V_{swing}} \approx 0.07C_{DAC} \quad (4)$$

where V_{REF} are assumed 1.8V and V_{swing} is assumed 0.8V. This value of C_{CAL} enables mismatch error up to 3σ to be corrected by calibration, so satisfactory yield can be achieved. We can see that C_{CAL} can be much smaller than C_{DAC}, therefore its noise contribution can be made negligible.

The Cal[*i*] and D[*i*] signals control if the *i*th DAC element is in calibration mode and the digital data applied to the *i*th DAC element, respectively. They are coming from flip-flops clocked by a digital clock which has rising edges in the middle of the clock phase Φ1 as can be seen in the timing diagram in Fig. 2. Fig. 3 shows the proposed control circuit that generates calibration control signals Cal[1]~Cal[*N+1*] and D[1]~D[*N+1*]. It consists of a shift register which is clocked by CLK_{CAL}, a clock generated by dividing the digital clock by 128 times. The shift register is filled by the value one from left to right, until the last register becomes one, when the reset signal is asserted, and all the resisters are reset to zero. The zero/one boundary determines which DAC element is chosen for calibration. The values stored in the shift register facilitate correct re-distribution of Din[1]~Din[*N*] to the remaining *N* DAC elements that are not chosen for calibration as shown in Fig. 3. Due to its regularity, this control circuit can be extended to any number of DAC elements with only linear increase in complexity.

The z-domain analysis of the calibration loop can be performed using charge conservation at the summing node of OTA_{CAL}:

$$(2V_{REF} + \frac{zV_{OC}}{A})(C_{DAC} - C_{REF}) - (V_{OC} + \frac{zV_{OC}}{A})C_{CAL} = V_{OC}(z-1)(1+\frac{1}{A})C_{HOLD} \quad (5)$$

where A is the DC gain of OTA_{CAL}. Combining (2) and (5), and assuming A>>1, the transfer function from capacitor mismatch to the error charge is given by

$$\frac{Q_E}{C_{DAC} - C_{REF}} = \frac{2V_{REF}(z-1)}{z-(1-C_{CAL}/C_{HOLD})}. \quad (6)$$

The stability condition is

$$C_{HOLD} > C_{CAL}/2. \quad (7)$$

Since C_{HOLD} should not be too small in order to guarantee stability as well as to reduce the voltage error from switch leakage current, it is implemented using PMOS gate capacitor to save die area. The gate is connected to the summing node of OTA_{CAL}, which has low common mode voltage, while the source, drain and bulk are connected to OTA_{CAL}'s output. Fig. 4 shows the schematic of OTA_{CAL}. Simple folded cascode OTA with PMOS input is used to set the summing node common mode voltage low so that channel is formed in the PMOS capacitor C_{HOLD}. Since each OTA_{CAL} is very small, it would be wasteful to implement SC common-mode feedback (CMFB) circuit for each one. Instead, triode NMOS transistors are used to set output common mode voltage near a desired value *vocm* through replica biasing.

III. Circuit Non-idealities

A. Switch Charge Injections

Most existing multi-bit DAC with analog background calibration, including [5-7], suffer from mismatch of charge injected by switch in each DAC element. A common structure that can be seen in these DACs is a hold capacitor and a switch per each DAC element that connects this hold capacitor to a shared reference. When the DAC element transitions out of calibration mode, this switch turns off, and injects a charge packet to the hold capacitor, corrupting the calibrated voltage. This charge is not guaranteed to be exactly the same for each DAC element because the switch transistor can have mismatch. Therefore the accuracy of existing analog calibrated DACs is often limited to about 14-bit [5-6].

An improved switching sequence and the use of switched-capacitor integrator in the calibration loop made

it possible to avoid this problem in our proposed structure. Shown in Fig. 1, the corresponding switches connecting each DAC element to the calibration reference are S4 and S5. As seen in the timing diagram in Fig. 2, when a DAC element transitions out of calibration mode, S4 and S5 turns off. Since S6 has been turned ON, and S7 has been turned OFF, before this happens, the charge injected toward the virtual ground by S4 and S5 will go to ground through S6 and will never reach C_{HOLD} because S7 is off. The voltage held on C_{HOLD} will therefore not be corrupted. Fig. 5 shows simulated waveform at the transition instant. Due to parasitic capacitance in parallel with switch S7, and the finite ON-resistance of S6, the injected charge from S5 will disturb the voltage at node Voc temporarily. But since there is no resistive path, charge held on C_{HOLD} never gets corrupted, and Voc soon settles to the correct voltage. S6 will stay ON and S7 OFF when the element is not under calibration, therefore exactly the same condition as that of clock phase Φ1 during calibration mode is maintained when V_{OC} is sampled.

When the element is under calibration, the sampling instant is determined by S8 since S6 remains OFF. There is no mismatch in charge injection because there is only one S8. Similarly, when the element is in use, the sampling instant is determined by S1, which is shared by all the DAC elements, so there is no charge injection mismatch as well. Charge injected by S3 when it turns off can never corrupt the transferred charge because S3 closes after the sampling instant.

B. Other Circuit Non-idealities

The op-amp OTA_{CAL} of each DAC element may have different offset. To prevent this from degrading the accuracy of calibration, the offset canceling integrator [8] is used. C_{OS} stores the op-amp offset during Φ1, effectively creating an offset-free virtual ground. Calibration should be repeated for each DAC element with an interval short enough such that the leakage current through switches, as well as offset drift of OTA_{CAL} cause negligible voltage change at V_{OC}. To reduce the effect of leakage the value of C_{HOLD} should be made large. Since the linearity of C_{HOLD} is not important they are implemented as PMOS gate capacitor to save die area. The PMOS gate is connected to the virtual ground which has lower common-mode voltage than the output. Complementary transmission gate is used for every switch since leakage by NMOS and PMOS to the substrate and n-well can cancel.

The DC gain of OTA_{CAL} becomes the only linearity limiter in our proposed method. By setting z to 1 in (5) we find the steady state error charge to be

$$Q_E = 2V_{REF}(C_{DAC} - C_{REF})\frac{(C_{DAC} - C_{REF} - C_{CAL})}{C_{DAC} - C_{REF} - C_{CAL}(1 - A)} \quad . \tag{8}$$

We can see from (8) that the mismatch error is attenuated by the DC gain of OTA_{CAL}, A.

IV. Design Example and Simulation Results

A 3-bit (N=7) switched capacitor DAC is designed in 0.18μm CMOS to be used as first stage multi-bit feedback DAC in a pipelined ADC with a 100MHz sampling frequency. C_{DAC} is 100fF, C_{CAL} is 40fF, and C_{HOLD} is approximately 230fF realized by PMOS gate capacitors. A mismatch with standard deviation of 0.1% is applied to all capacitors; and threshold voltage mismatches with standard deviation given by

$$\sigma V_{th} = \frac{6[\mathrm{mV}\mu\mathrm{m}]}{\sqrt{\mathrm{WL}[\mu\mathrm{m}^2]}} \tag{9}$$

are applied to all switch transistors and opamp input transistors. The frequency of the calibration clock CLK_{CAL} is 1/128 of the sampling clock frequency. Each OTA_{CAL} dissipates about 200μA, and the transconductance is 0.5mS for each side. This value is not enough for the output to settle completely within half clock period (5ns) during the calibration mode, when the load is $C_{CAL}+(C_{HOLD}||2C_{DAC})$. However, since calibration for each DAC element will last for 128 sampling clock period, eventually, the voltage step will be very small. Incomplete but mostly linear settling causes the effective values of C_{DAC}, C_{REF} and C_{CAL} in equations (5)~(8) to be smaller than their nominal values. We can see that stability condition is still satisfied and residue error is still in the order of 1/A. To verify this argument, transient simulation is done with both a 10MHz clock frequency, when OTA_{CAL} completely settles within half sampling period, and the 100MHz clock frequency. No difference was seen in the final simulation results.

In order to only observe the nonlinearity caused by element mismatch, OTA1 is realized as an ideal transconductor. The rest of the circuit is entirely simulated with transistor schematic. A ramp digital sequence is applied as input to the DAC and the difference between the DAC output voltage and the ideal output voltage (which corresponds to the INL) is plotted versus time in Fig. 6. We can see that the INL improves by more than 2 orders of magnitude (40dB) after 7 calibration clock cycles (896 sampling clock periods). Larger value of C_{HOLD} can always be used to reduce voltage drop due to leakage current, so that better linearity can be achieved. But even for the moderate value (230fF) as in this example, 15-bit linearity is achieved.

References

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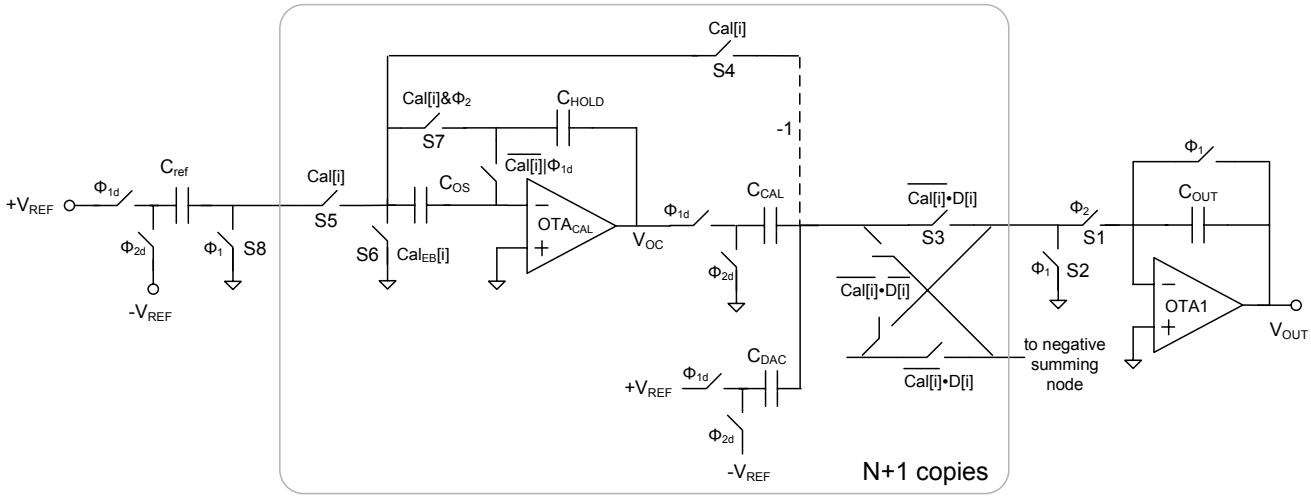

Fig. 1. Single-ended view of the proposed switched capacitor DAC with background calibration

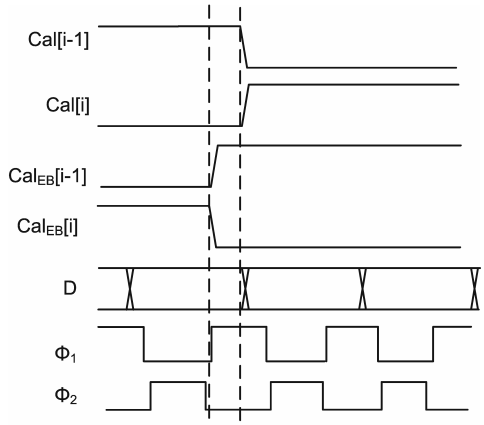

Fig. 2. Timing diagram of the clock and control signals

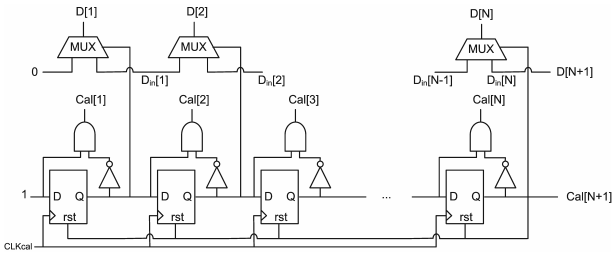

Fig. 3. Proposed background calibration control circuits

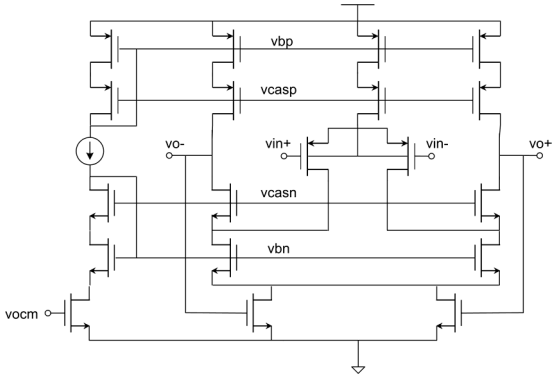

Fig. 4. Schematic diagram of OTA_{CAL}

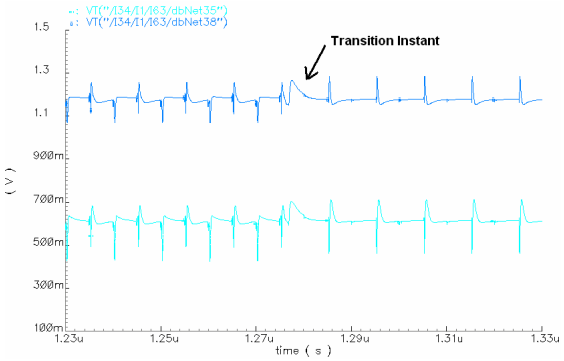

Fig. 5. Simulated waveform of Voc+ and Voc- during the transition out of calibration mode

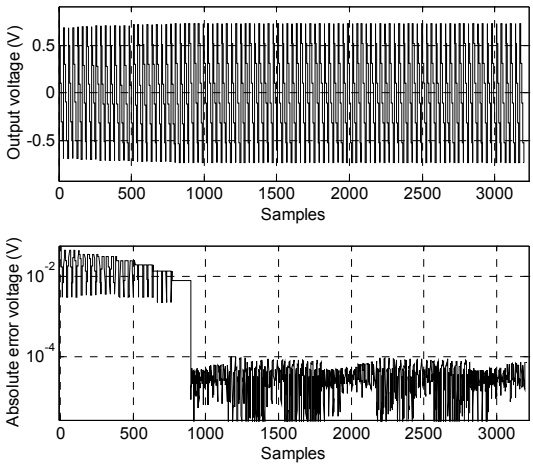

Fig. 6. Simulated output voltages and error voltages vs. time