

Aperture Uncertainty and ADC System Performance

by Brad Brannon

Aperture Uncertainty

One of the key concerns when performing IF sampling is that of aperture jitter or aperture uncertainty. The terms aperture jitter and aperture uncertainty are frequently interchanged in text. In this application, they have the same meaning. Aperture uncertainty is the sample-to-sample variation in the encode process. Aperture uncertainty has three residual effects: the first is an increase in system noise, the second is an uncertainty in the actual phase of the sampled signal itself and third is intersymbol interference. To achieve required noise performance, aperture uncertainty of less than 1 ps is required when IF sampling. In terms of phase accuracy and intersymbol interference, the effects of aperture uncertainty are small. In a worst case scenario of 1 ps rms at an IF of 250 MHz, the phase uncertainty of error is 0.09 degrees rms. This is quite acceptable even for a demanding specification such as GSM. The focus of this analysis will therefore be on overall noise contribution due to aperture uncertainty.

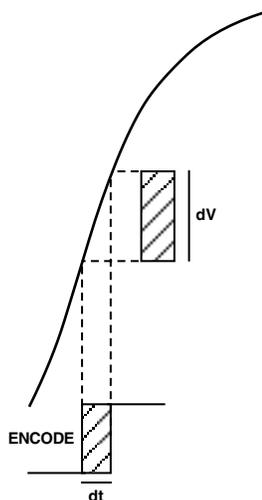


Figure 1. RMS Jitter vs. RMS Noise

In a sine wave, the maximum slew rate is at the zero crossing. At this point, the slew rate is defined by the first derivative of the sine function evaluated at $t = 0$.

$$v(t) = A \sin(2\pi ft) \quad \frac{d}{dt} v(t) = A 2\pi f \cos(2\pi ft) \quad (1)$$

evaluated at $t = 0$, the cosine function evaluates to 1 and the equation simplifies to:

$$\frac{d}{dt} v(t) = A 2\pi f = t_{JITTER} \quad (2)$$

The units of slew rate are volts per second and yields how fast the signal is slewing through the zero crossing of the input signal. In a sampling system, a reference clock is used to sample the input signal. If the sample clock has aperture uncertainty, an error voltage is generated. This error voltage can be determined by multiplying the input slew rate by the jitter.

$$V_{ERROR} = \text{Slew Rate} \times t_{JITTER} \quad (3)$$

By analyzing the units, it can be seen that this yields unit of volts. Usually, aperture uncertainty is expressed in seconds rms and, therefore, the error voltage would be in volts rms. Additional analysis of Equation 3 shows that as analog input frequency increases, the rms error voltage also increases in direct proportion to the aperture uncertainty.

Contribution to Overall System Performance

In IF sampling converters, clock purity is of extreme importance. As with the mixing process, the input signal is multiplied by a local oscillator or in this case, a sampling clock. Since multiplication in time is convolution in the frequency domain, the spectrum of the sample clock is convolved with the spectrum of the input signal. Since aperture uncertainty is wideband noise on the clock, it shows up as wideband noise in the sampled spectrum as well. And since an ADC is a sampling system, the spectrum is periodic and repeated around the sample rate. This wideband noise therefore degrades the noise

floor performance of the ADC. The theoretical SNR for an ADC, as limited by aperture uncertainty, is determined by the following equation.

$$SNR = -20 \log [(2 \pi f_{analog} t_{JITTER\ rms})] \quad (4)$$

If Equation 4 is evaluated for an analog input of 201 MHz and 0.7 ps rms "jitter," the theoretical SNR is limited to 61 dB. Therefore, systems that require very high dynamic range and very high analog input frequencies also require a very low jitter encode source. When using standard TTL/CMOS clock oscillators modules, 0.7 ps rms has been verified for both the ADC and oscillator. Better numbers can be achieved with low noise modules.

When considering overall system performance, a more generalized equation may be used. This equation builds on the previous equation but includes the effects of thermal noise and differential nonlinearity.

$$SNR = -20 \log \left[(2 \pi f_{analog} t_{JITTER\ rms})^2 + \left(\frac{1+\epsilon}{2^N} \right)^2 + \left(\frac{V_{noise\ rms}}{2^N} \right)^2 \right]^{1/2} \quad (5)$$

- f_{analog} = analog IF Frequency
- $t_{JITTER\ rms}$ = aperture uncertainty
- ϵ = average DNL of converter (~ 0.4 LSB)
- $V_{noise\ rms}$ = thermal noise in LSBs
- N = number of bits

Although this is a simple equation, it provides much insight into the noise performance that can be expected from a data converter.

Measurement of Sub-Picosecond Aperture Uncertainty

Aperture uncertainty is easily measured by looking at degraded SNR performance as a function of analog input frequency. Since SNR degrades as analog input frequency increases due to jitter, two FFTs are required for the calculation. The first FFT should be done at a sufficiently low analog frequency where the effects of aperture uncertainty are negligible. Record the SNR excluding all harmonics and higher order spurs. Then solve Equation 5, above, for general converter performance by assuming that thermal noise is rolled up into the quantization noise and jitter is neglected. This gives the equation below.

$$\epsilon = 2^N \times 10^{\frac{-SNR}{20} - 1} \quad (6)$$

- SNR is the low frequency SNR
- N is the number of converter bits
- ϵ = average DNL (+ thermal noise)

Then an FFT is done at very high frequency. The high frequency should be chosen to be near the 3 dB bandwidth of the converter. Again, the SNR without harmonics should be measured.

At this high frequency, we can assume that jitter is a contributor to noise. From the previous data measurement we know the average quantization and thermal noise; we can solve the general form equation for jitter as shown.

$$t_{JITTER\ rms} = \frac{\sqrt{\left(10^{\frac{-SNR}{20}} \right)^2 - \left(\frac{1+\epsilon}{2^N} \right)^2}}{2 \pi f_{IF}} \quad (7)$$

- SNR is the high frequency SNR
- N is the number of converter bits
- ϵ = average DNL from above and thermal noise
- f_{IF} is the IF analog input frequency

Putting the Calculations to the Test

The following data was collected using the AD9042ST/PCB evaluation board. No modifications were made. The clock oscillator (M1280, manufactured by MF Electronics) supplied with the evaluation board was used to generate the encode signal which was delivered to the AD9042 differentially via a transformer (Mini-Circuits T1-1). The analog input was generated by a Rohde & Schwarz synthesizer. For more information about the evaluation board, please see the AD9042 data sheet.

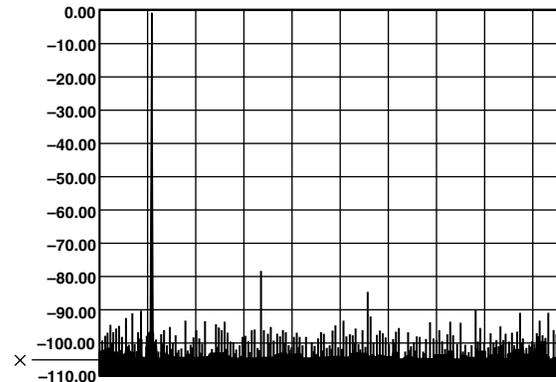


Figure 2. 2.3 MHz FFT

Figure 2 is a 16K FFT of the AD9042 sampling a 2.3 MHz sine wave at 40.96 MSPS. Since we must exclude higher order harmonics from the SNR calculation, x represents the unintegrated noise floor, or the mean noise floor. Instead of integrating all of the noise spikes, this number is summed across the entire spectrum, thus eliminating the higher (and lower) order harmonics. Using Equation 8:

$$SNR = -(-108 + 10 \log (8192)) \quad (8)$$

SNR is found to be 69 dB. When this is used to solve Equation 6 for ϵ the average DNL (and thermal noise) for this converter is 0.4533 LSBs.

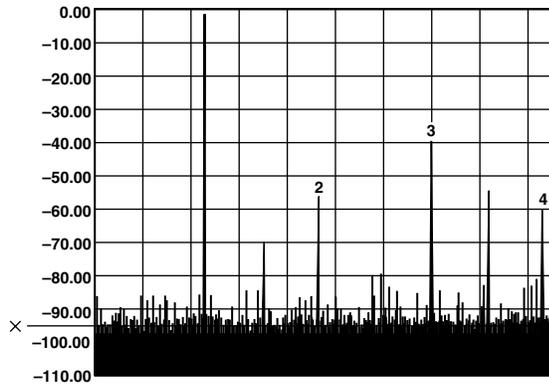


Figure 3. 201 MHz FFT

Next, the degradation in SNR must be found as a function of analog input frequency. Figure 3 is the same AD9042 and clock, but running an analog input frequency of 201 MHz. This time the unintegrated noise floor has risen by almost 10 dB. Integrating with this value of x yields an SNR of 60 dB. Using this SNR and the previous solution for ϵ , the jitter can be found as follows using Equation 7:

$$t_{JITTER\ rms} = \frac{\sqrt{\left(10^{\frac{-60}{20}}\right)^2 - \left(\frac{1 + 0.4533}{2^{12}}\right)^2}}{2\pi \cdot 201 \times 10^6} = 0.74\ ps\ rms \quad (9)$$

Therefore, the combined aperture uncertainty for the AD9042 plus the clock oscillator is found to be less than three quarters of a picosecond rms. At this time, it is not possible to determine which part is from the ADC and which from the clock oscillator; however, these simple measurements indicate that it is possible to measure very small aperture uncertainty numbers using readily available hardware and simple numeric calculations.



Figure 4. Aperture Uncertainty Measurement Setup

Many applications require that a master clock be distributed to many different sources. Many systems have multiple ADCs such as cellular basestations or ultrasound equipment. The question quickly arises, however, how much jitter is introduced into a system when placed in a distribution system. The first option in distributing an ADC clock is to use logic gates to fan out the encode signal, but this rapidly increases the amount of jitter introduced into the system.

By using the technique described above, the jitter per gate (74xx00) for several logic families was measured and summarized below.

	Jitter	Equivalent NF
74LS00	4.94	28
74ACT00	0.99	15
74HCT00	2.20	21.84

Table I shows that the 74ACT00 gate delivers the lowest jitter of almost 1 ps rms. In many applications, even this is unacceptable. For receiver applications, the equivalent noise figure is shown for reference (valid at 201 MHz analog input only). Thus when using logic gates for ADC clock distribute, they must be used minimally or not at all.

Recent ADC developments require differential clock drive. With this comes the ability to drive the encode with a sinusoidal signal instead of a square wave.

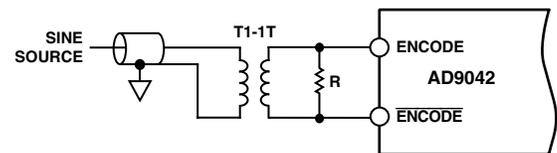


Figure 5. Transformer Differential Encode

As shown above, a sine source can be distributed to encode the ADC. Sine sources can easily be distributed using power dividers and transformers to match impedances. Since ADC encode pins are high impedance, very little power is required to encode the devices and thus, when driving multiple devices, low encode drive power is required. Since the sine source is spectrally pure, fewer problems can be expected in receiver applications with harmonics of the ADC encode clock.

The chart following, Figure 6, is a useful guide for quickly determining jitter requirements based on analog input frequency and converter bits. This chart is from Analog Devices' publication, High Speed Design Seminar (ISBN 0-916550-07-9).

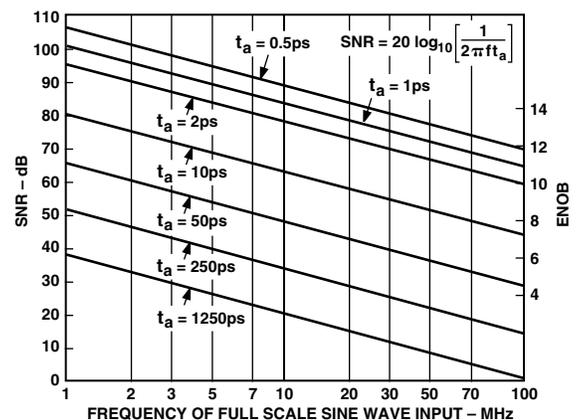


Figure 6. Signal-to-Noise Ratio Due to Aperture Jitter