ECE 1352F
Reading Assignment

Mismatch Shaping for Multibit ΔΣ ADCs

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Abstract - **Delta-sigma (ΔΣ) modulation is a popular technique for making high resolution analog to digital and digital to analog converters (ADC and DAC) despite a variety of circuit imperfections. Multibit feedback DACs in ΔΣ ADCs offer significant advantage over a traditional single bit quantizers. The advantages of multibit quantizers are discussed and the it is shown that mismatch shaping can be used to reduce the errors caused by mismatches in the feedback DAC of a ΔΣ ADC.**

I. Introduction

One technique for realizing high resolution ADCs and DACs is delta-sigma (ΔΣ) modulation. The significant advantage of this scheme is that signals are converted using a low resolution quantizer and the precision of the analog circuitry is usually much less than the resolution of the overall converter. However, this comes at the expense of sampling the signal faster than is required. The side benefit of oversampling is that the antialias filter is much simpler. The most common ΔΣ modulator currently in use is the binary low-pass modulator. It is typically used in the audio field, to quantize low-pass signals with high accuracy [4].

In this paper DS ADCs with multibit quantizer is examined. The effect of mismatch in the feedback DAC is studied. Section II presents a brief background on ΔΣ modulator theory. Section III discusses the advantages of using a multibit quantizer in the feedback path of ΔΣ ADC. Section IV examines the effect of DAC mismatch on ADC performance and introduces the various mismatch shaping techniques used to reduce the problem. Section V compares the various mismatch shaping techniques and Section VI summarizes this paper.

II. Background

The basic principal behind ΔΣ modulation is that of feedback and filtering around a low-resolution quantizer [1]. Fig. 1 shows a general block diagram of a ΔΣ modulator. The resolution of the quantizer is usually much less than the resolution of the overall converter and can be just a simple comparator and a single bit DAC. The loop filter is digital in the case of a DAC and analog in an ADC. The loop transfer functions L_1 and L_0 have very high gain in a narrowband (ideally infinite gain at frequencies for which $H = 0$). Due to the negative feedback action of the loop, the actual resolution after filtering is much better than the resolution of the quantizer. This is accomplished by oversampling the input and feeding back the output from the quantizer to a resonator circuit. If the system is stable, the frequency component of the error at the loop filter's resonant frequency must be small. Therefore the output closely represents the input around a narrow frequency band for which the loop filter possesses high gain.

The modulator consists of two sections: a linear block (the loop filter) and a nonlinear block (the quantizer). Assuming for now that the loop filter is a discrete-time filter, the output of the linear block can be written as

$$Y(z) = L_0(z)U(z) + L_1(z)V(z) \qquad (1)$$

Modeling the quantizer in Fig. 2 as an additive white noise source, (i.e. $V(z) = Y(z) + E(z)$), (1) can be rearranged to give the output of the modulator in terms of its input and the error signal

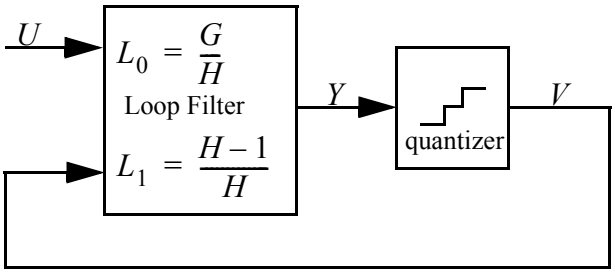

Fig 1. A general block diagram of a ΔΣ modulator.

$$V(z) = G(z)U(z) + H(z)E(z) \quad (2)$$

With appropriate choice of the loop filters, $G(z)$, the signal transfer function (STF) will pass signals in a certain frequency band, while $H(z)$, the noise transfer function (NTF) will attenuate the error signal in that band, and so the signal can be separated from the noise by a digital filter. Thus, the output can faithfully represent the input in a narrowband where $H(z)$ is small. Note that the poles of L_1 are the zeros of the $H(z)$.

Oversampling increases signal to noise ratio (SNR) by spreading a fixed quantization noise power over a bandwidth that is larger than the signal bandwidth. Noise shaping or modulation further attenuates this noise in the band-of-interest and amplifies it outside the passband. This process can be viewed as pushing quantization noise power from the signal band to other frequencies.

The two most important parameters in determining the performance of ΔΣ modulator are its oversampling ratio (OSR) and NTF. By increasing OSR, in-band noise is reduced and hence SNR is increased. The NTF determines the in-band quantization noise attenuation, thus the maximum SNR that the modulator can achieve for a given value of OSR. $H(z)$ must be designed to minimize the in-band noise under two constraints: one for causality and one for stability. The loop around the quantizer cannot be delay-free, so $H(z)$ - 1 must be strictly causal (i.e. first impulse-response coefficient zero). This constraint forces

$$\lim_{z \to \infty} H(z) = 1 \quad (3)$$

which indicates that $H(z)$ can not be set to zero everywhere. Making $H(z)$ small in-band forces it to be greater than unity out-of-band [1].

The stability of single bit ΔΣ modulators is a much less understood problem [1], [2]. Ensuring that $H(z)$ is stable does not guarantee that the modulator will be stable. However, according to Lee's rule-of-thumb [3], for binary modulators, stability is ensured if the following constraint is met

$$|H(e^{j\omega})| < 2 \qquad -\pi \le \omega < \pi \tag{4}$$

This rule is approximate in nature and it is possible to find stable binary modulators for which Lee's rule is violated. Since stability of a ΔΣ modulator is an unsolved problem, simulation of the non-linear system with large inputs is the only way to ensure that the modulator will be stable.

Note that the loop filters (L_1 and L_2) can be implemented using either discrete-time filters such as switched-capacitor (SC) or it can be implemented using continuous-time filters, for example using LC, g_m-C or RC filters. One of the main advantages of a continuous-time loop filter is that because the sampling operation is done at the output of a continuous-time loop filter, alias frequencies are suppressed by the loop filter [8]. To see this consider, the following: suppose a signal at an alias frequency of f_0 (e.g. $f_s + f_0$) is applied at the input. Now if this system had no anti-alias properties, that signal would be aliased back to f_0 at the feedback DACs (the quantizer is clocked) and because the filter has very high gain at f_0, the system would become unstable. Therefore if the system is stable then no alias frequency can be fed back through the feedback DACs. A further advantage of a continuous-time modulator is that sampling errors are noise-shaped along with the quantizer errors and thus the requirements of the sample and hold block is reduced.

III. multibit Quantization

ΔΣ ADCs based on one bit quantizers have been widely used to create highly linear converters [4]. Single bit conversion is desirable because a single bit DAC is inherently linear. However, ΔΣ ADCs with one bit feedback DAC generally require a large oversampling ratio to achieve high SNR. That is because the NTF can not be made arbitrarily small in-band and still be stable (i.e. meet the constraint given in (4)). However, by using a multibit feedback DAC in the ΔΣ ADC, the restriction given by Lee's rule can be ignored to achieve a more optimized NTF. A further

improvement in SNR comes from the fact that the power of the quantization noise, $E(z)$, will also decrease with multibit quantizer. For an N bit quantizer, this translates into about $6(N\text{-}1)$ dB improvement over a binary modulator with the same NTF. Thus for a given order and OSR, a multibit modulator will have a much higher SNR than a binary modulator. As an example, it was shown in [5] that a binary fifth order modulator can achieve a maximum SNR of 60 dB while a ΔΣ ADC with an eight level quantizer can achieve 108 dB SNR for the same given OSR and modulator order. This was accomplished by designing a more aggressive NTF with a larger out-of-band gain and therefore a lower in-band gain. Another advantage of a multibit ΔΣ modulators is that its behavior more closely follows that predicated by the linearize model. Consequently, the stability of higher order modulators using multibit quantizers is more accurately predicted by the linearized model [4].

IV. Noise Caused by DAC Element Mismatch

One of the main drawbacks of using a multibit feedback DAC is that the DAC can not be made perfectly linear since it is impossible to manufacture DACs with exactly equal step size. This imperfection causes non-linear behavior of the DAC output. The problem is made worse by the fact that any error introduced by the feedback DAC will translate directly into errors for the overall converter [2]. The linearity of a ΔΣ ADC is also no better than that of its multibit internal feedback DAC. To illustrate this, consider the modulator shown in Fig. 2. Assuming the error introduced by mismatches in the feedback DAC can be modeled as additive white noise, the linear model of a multibit ΔΣ modulator is

$$V = GU + HE + (H-1)E_{DAC} \qquad (5)$$

where $(H-1)E_{DAC} \approx -E_{DAC}$ in the band-of-interest. Thus, in-band noise will be dominated by

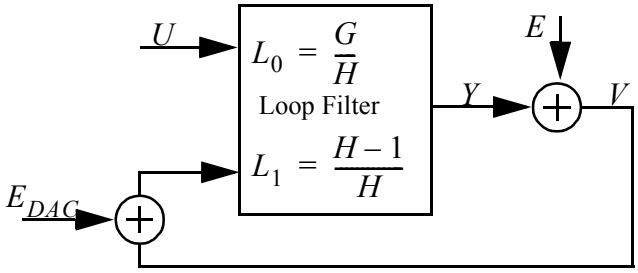

Fig 2. A general block diagram of a ΔΣ modulator with DAC error.

the DAC noise. However, given the huge increase in SNR that is possible with the use of a multi-bit feedback DAC has led to several schemes whereby the DAC errors are pushed out-of-band. To accomplish this task, the feedback DAC is constructed from identically sized unit elements. The DAC elements are then selecting in such a way that the non-linear error is randomized and moved out-of-band so that on average the error caused by element mismatch is canceled. The following section will discuss three such selection schemes.

A. Data Weighted Averaging

One common algorithm for reducing the effect of DAC error is the data weighted averaging (DWA) scheme [7]. The fundamental idea of DWA is to use all the elements at the maximum possible rate while ensuring that each element is used the same number of times. The DAC elements are chosen in a rotating fashion. A pointer is used to remember the last selected element and the next set of elements are chosen starting from that point. A block diagram of DWA is shown in Fig. 3. Fig. 4 shows an example of the resulting element usage pattern.

DWA operation is equivalent to differentiating a signal related to the integral non-linearity of the DAC. To illustrate this point, consider the following: DWA algorithm can be conceptually viewed as differentiating the output of the integral of the a non-ideal by infinite element DAC (see Fig. 5). The result of this operation is that the noise at the output of the DAC will be shaped by a

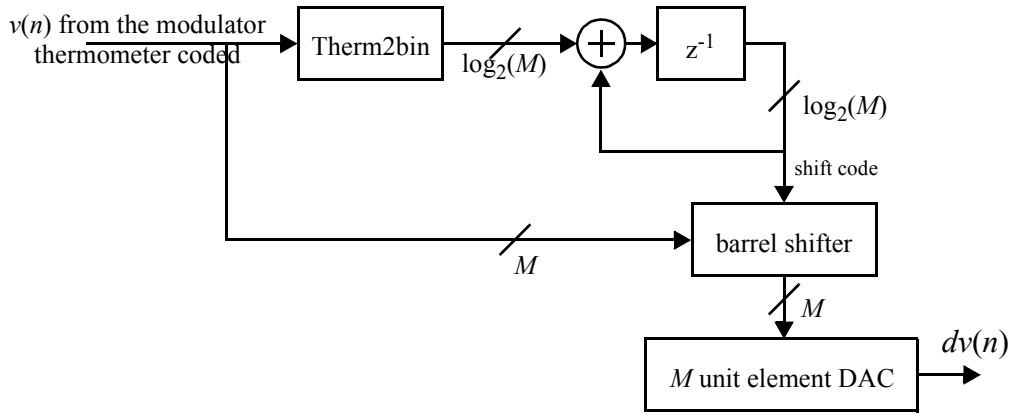

Fig 3. Block diagram of a DWA selection algorithm

first order function, i.e. $dV = V + (1 - z^{-1})E_{DAC}$. Therefore, DWA is equivalent to first order mismatch shaping, i.e the DAC noise is shaped by a $1 - z^{-1}$ transfer function and it has a -20 dB/ decade slope in the low frequency band.

B. General Mismatch Shaping Algorithm

The performance of DWA can be improved upon by using a more complex structure to reduce the in-band DAC noise. Fig. 6 shows a general block diagram of a mismatch shaping DAC that was described in [6]. The basic principal behind the mismatch shaping algorithm is the same as that behind the ΔΣ modulation; feedback and filtering around a low resolution quantizer. The output of the modulator which produces $M + 1$ quantization levels is fed into the element selection logic. At each time step n, the vector quantizer determines which $v(n)$ of the M unit elements will be

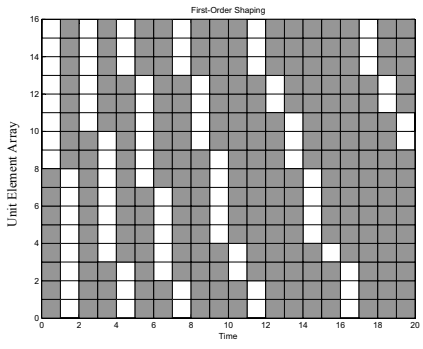

Fig 4. Element usage pattern of DWA.

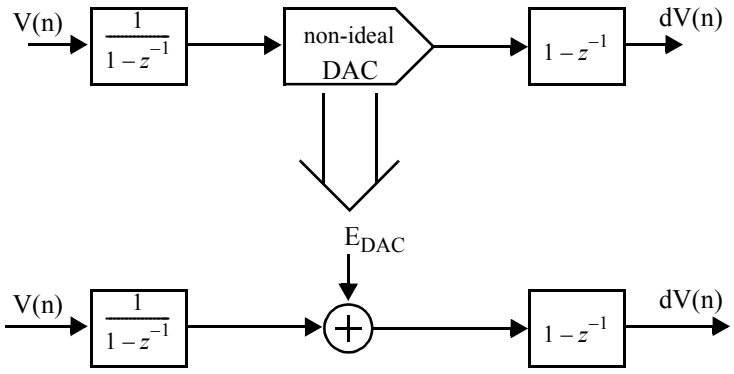

Fig 5. A conceptual diagram of the DWA algorithm.

used to produce the analog output value. This decision is based on the required element usage $v(n)$ and the content of the vector $\boldsymbol{sy}(n)$ (vectors are shown in bold). The goal of the vector quantizer is to keep the loop stable by minimizing $\boldsymbol{se}(n)$. For example, this can be accomplished by first choosing those elements in $\boldsymbol{sy}(n)$ vector that have a high value. This operation requires the need for a sorting operation. The output of the element selection logic is $\boldsymbol{sv}(n)$, a 1 x M vector containing $v(n)$ ones and M-$v(n)$ zeros. Each unit DAC element is controlled by a specific bit in the ***sv*** vector. The output of the DAC will be the analog version of the $v(n)$ plus an error term due to mismatch. The function of the element selection logic is to select elements in such a way that the mismatch error term is noise shaped. This is done by feeding back the error term ***se*** through an array of filters to form the subsequent sample of ***sy***. It was shown in [6] that the output of the DAC can be expressed as

$$DV(z) = kV(z) + H_2(z)DE(z) \qquad (6)$$

where k is the average element value, $V(z)$ is the output of the modulator, $DE(z)$ is the error signal introduced by element mismatch (i.e. the difference between the actual value of the element and the average value of all the elements), and $H_2(z)$ is the mismatch transfer function (MTF). Eqn. (6) shows that the DAC errors are shaped by the MTF, provided that the ***se*** signal is bounded. The stability of the mismatch shaping logic is an unsolved problem, and so simulations

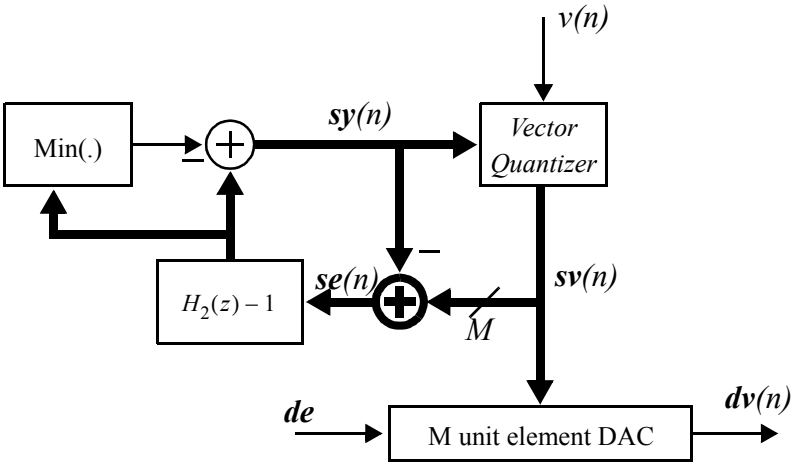

Fig 6. Generic element selection logic.

must be used to verify its stability.

Fig. 7 shows the simulated output spectra of a third-order 17 level modulator with a tone input. With an ideal feedback DAC, the performance of the modulator is 118 dB. With 1% mismatched DAC elements the SNR is degraded by less than 7 dB with a second order MTF. A first order MTF would require mismatch errors of less than 0.2% and with no mismatch shaping the require mismatch is less than 0.002% to achieve the same SNR[5]. The following section will examine the effect of DAC errors in continuous-time ADCs.

C. Mismatch Shaping for Continuous-Time Modulators

One of the main disadvantages of a continuous-time ΔΣ ADC is that it is sensitive to the DAC output over the entire feedback period, unlike a discrete time implementation which relies only on the final settled output value of the feedback DAC. In this case, both static and dynamic DAC errors degrade system performance. The two previously discussed mismatch shaping techniques have focused solely on reducing the static errors of the DAC. Dynamic DAC errors are caused by non-complementary rise/fall times. Although a DAC with a differential output stage will ideally have perfectly matched rise and fall dynamics, in practice due to device mismatch the rise/fall

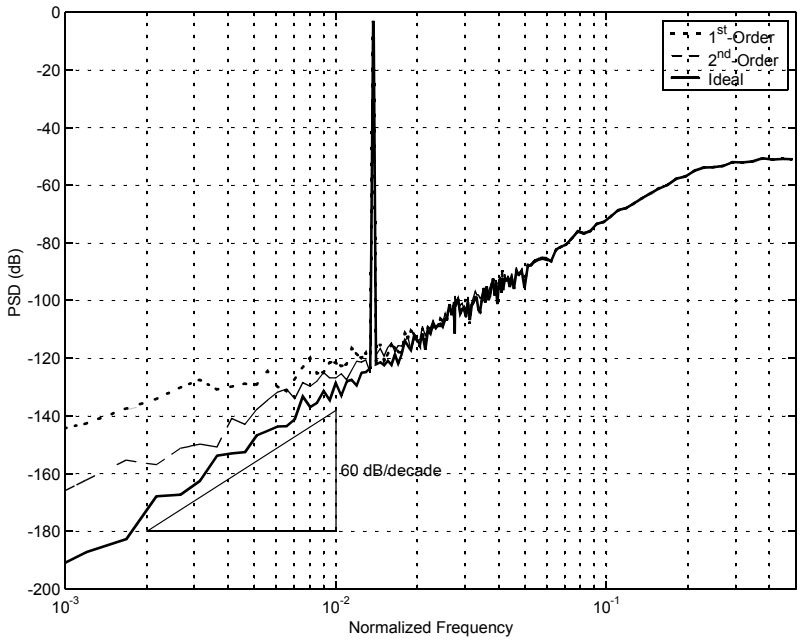

Fig 7. Output spectra for a third order lowpass modulator with 1% element mismatch

dynamics will not be perfectly matched and so the DAC will have dynamic errors as well as static mismatch errors associated with it. One way of reducing the dynamic errors, is to modify the vector quantizer shown in Fig. 6 so that the number of switching events per clock period is constant. Thus, non-complementary switching dynamic amount to the addition of a periodic signal to the DAC output. Since the error signal is repeated at every clock cycle, the output spectrum is corrupted with a DC offset and harmonics of the clock. Depending on the application of the ADC, this may or may not be a problem. More detailed description of the modified mismatch shaping algorithm is given in [5].

V. Future Developments

For high OSR, second order MTF offers a significant advantage over first order MTF in reducing the error caused by DAC element mismatch. Although second order MTF is possible with the system shown in Fig. 6, it requires a significant increase in hardware when compared to a DWA scheme. Furthermore, the output of the element selection logic $\boldsymbol{sv}(n)$, needs to be computed in less

than one clock cycle so that it can be used in the feedback path of a ΔΣ ADC. This extra requirement, will likely mean that second order mismatch shaping is unlikely to be used in high speed ΔΣ ADC application. Furthermore, for low OSR, the effectiveness of the second order algorithm in suppressing the errors is no better than the first order algorithm [9]. Therefore, the simple DWA scheme will likely be the dominant mismatch shaping algorithm used in high speed multibit ΔΣ ADCs.

Mismatch shaping can also be extend to bandpass and quadrature ΔΣ modulators. In [10], a mismatch shaping algorithm for quadrature modulators was been developed. However, the algorithm presented in [10] is complex and therefore not very suitable for high speed applications, further work in this area is necessary. The concept of mismatch shaping can also be applied to other types of converters. For example, in [11], a mismatch algorithm was used to increase the SNR and the linearity of an oversampled pipelined ADC.

VI. Conclusion

A brief background on ΔΣ modulation was given in Section II. Section III examined the behavior of a ΔΣ ADC with a multibit feedback DAC. Three mismatch shaping techniques were introduced in section IV to reduce the degradation in SNR caused by DAC mismatch. Section V compared the various mismatch shaping algorithms and drew conclusion about the future direction of the field.

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