

# MULTIBIT QUADRATURE SIGMA-DELTA MODULATOR WITH DEM SCHEME

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## ABSTRACT

A simple dynamic element matching (DEM) scheme for sampled data systems is presented. The scheme is suitable for Switch-Capacitor (SC) or Switch-Current circuits. The DEM scheme eliminates the mirror spectral image around  $\pm Fs/4$ , where  $Fs$  is the sampling frequency, while generally introducing a more benign self-image. The scheme is suitable for quadrature SC Band-Pass (BP)  $\Sigma\Delta$  modulators with a centre frequency at  $Fs/4$  or  $-Fs/4$ , where it can minimize the quantization noise mirror image and where the signal mirror image can be suppressed. Furthermore, a quadrature mismatch noise shaping method that can be used with this DEM scheme is introduced.

## 1. INTRODUCTION

A quadrature BP  $\Sigma\Delta$  modulator can provide a larger SNR than a pair of real BP  $\Sigma\Delta$  modulators of similar complexity [1],[2], but it suffers from path mismatch which causes both signals and quantization noise in the mirror image band to alias into the desired signal band, thus degrading the SNDR of the converter. Section 2 presents a simple DEM scheme to compensate for path mismatch that is suitable for single bit quadrature  $\Sigma\Delta$  modulators. The DEM scheme reduces the amount of mirror image band quantization noise aliased in the signal band. It also removes the mirror signal image alias, at the expense of introducing a self-image component. A particular SC topology that suppresses both the mirror image alias and the self-image component is identified. In section 3, an extension of this technique to multibit converters is introduced. Finally, in section 4 the effectiveness of the scheme is illustrated with behavioural simulations.

## 2. DEM SCHEME

To illustrate the effect of path mismatch, let's consider a unity gain complex path with a mismatch coefficient  $\delta$  (Fig.1 a). Its output is readily found as:

$$y(n) = x(n) + \delta x(n)^* \quad (1)$$

where \* indicates conjugation. If  $X(f)$  is the Fourier transform of  $x(n)$ , then  $X(-f)^*$  is the Fourier transform of its conjugate  $x(n)^*$ . The mismatch introduces, therefore, a noise floor which has the power spectral envelope of  $X(f)$  mirrored around  $f=0$  and scaled by the mismatch coefficient  $\delta$ . This is particularly undesirable for a quadrature BP  $\Sigma\Delta$  modulator with a centre frequency at  $+Fs/4$ . The ideal shaped quantization noise has very little power (a deep notch) at  $+Fs/4$ , but very strong components at  $-Fs/4$ . As shown by (1), mismatch mirrors some of the power of the quantization noise from  $-Fs/4$  to  $Fs/4$  filling the notch, as shown in Fig.4.

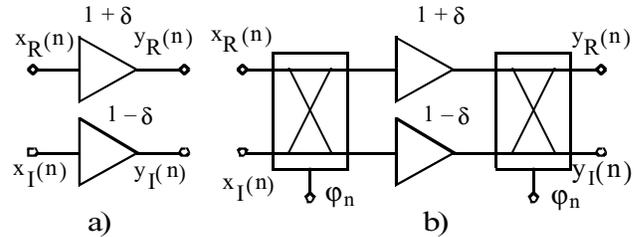


Fig.1:unity gain with mismatch (a) and with swappers(b).

In a sampled data system, a simple scheme which dynamically matches the real and imaginary paths consists of alternating each channel element between both paths. This can be implemented using swappers. Fig. 1b) shows the gain element with mismatch of Fig.1 a) preceded and followed by swappers.  $\phi_n$  is the sampling clock. For clock cycle index  $n$  even, the swappers are just a through connection, (that is the real input of a swapper is connected to its real output, and its imaginary input is connected to its imaginary output), while for clock cycle index  $n$  odd a swapper connects its real input to its imaginary output, and its imaginary input to its real output. This results in the following input-output relationship for the system of Fig. 1b):

$$y(n) = x(n) + \delta (-1)^n x(n)^* \quad (2)$$

The multiplication with  $(-1)^n$  is equivalent to mixing with a cosine at a frequency  $Fs/2$ , which frequency shifts the mismatch introduced noise by  $\pm Fs/2$ .

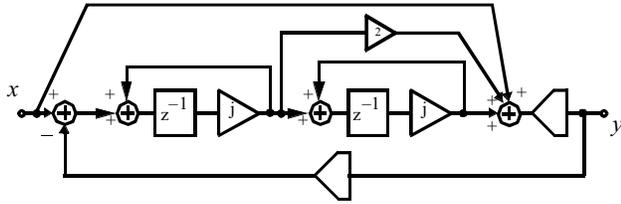


Fig.2: 2<sup>nd</sup> order quadrature BP ΣΔ modulator.

This property can be used to mitigate the impact of the quantization noise mirror image in a quadrature BP ΣΔ modulator centred at  $F_s/4$ . Let's consider the case where  $x(n)$  is shaped quantization noise with a notch at  $F_s/4$  and strong components at  $-F_s/4$ . Then the power spectrum of  $x(n)^*$  has very little power at  $-F_s/4$  (a deep notch) and by frequency shifting it by  $\pm F_s/2$  this notch is moved back to the wanted frequency of  $F_s/4$ .

The above DEM scheme has been applied to the 2<sup>nd</sup> order quadrature BP ΣΔ modulator of Fig. 2 resulting in the modulator topology of Fig. 3 using a two step procedure. First, every unity gain  $G$  block with potential mismatch has been inserted between two swappers. Second, the following functional identities have been used to reduce the number of swappers: a) the cascade of two swappers driven by in phase clocks is equivalent to a straight connection; b) the cascade of two swappers driven by opposite phase clocks is equivalent to a constantly swapped connection; c) a swapper can be moved across an ideal delay element by inverting its clock phase; d) a swapper in front of an ideal  $j$  multiplier can be moved after the  $j$  multiplier inserting a block that performs a sign inversion when the swapper clock is high. We notice that  $j$  multipliers can be implemented without error in differential systems.

Fig. 4 shows the averaged output spectrum of the

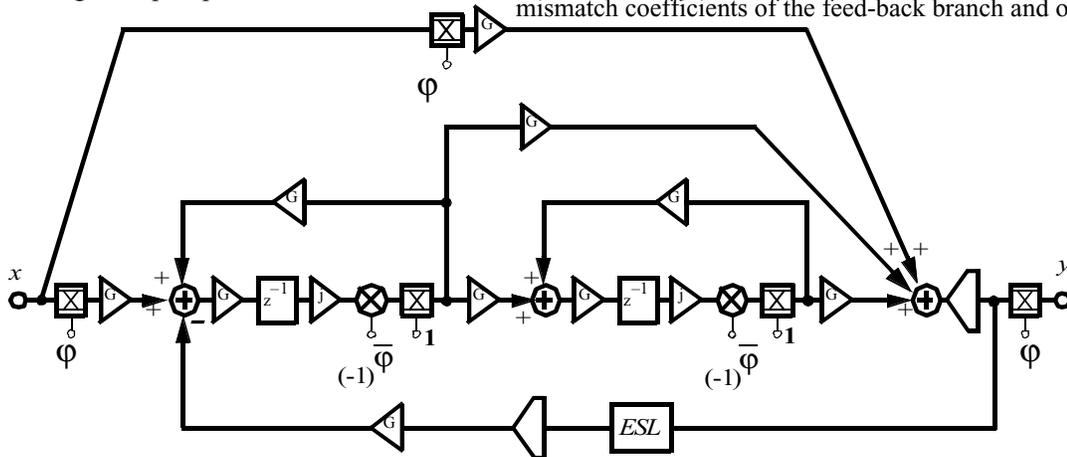


Fig.3: 2<sup>nd</sup> order quadrature BP ΣΔ modulator with DEM.

modulator of Fig.3 where all the mismatch coefficients have been set to 1%, while everything else is kept ideal. The DEM scheme results in a significant SNR improvement. The residual mismatch mirrored noise that still fills the notch is caused by second order effects. It is shown to decrease considerably as the order  $m$  of the ΣΔ

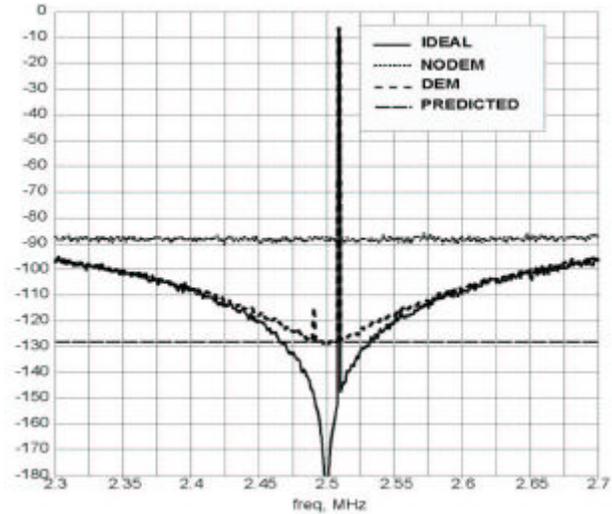


Fig.4: output spectrum, ideal, w/wo DEM and predicted.

modulator increases, according to:

$$N_{QR} = \prod_{i=1}^m \left( \delta_{yi} + \delta_{ui} \right)^2 N_Q \quad (3)$$

where  $N_Q$  is the power spectral density (PSD) of the quantization noise,  $N_{QR}$  is the PSD of the residual aliased quantization noise,  $\delta_{yi}$  and  $\delta_{ui}$  are respectively the mismatch coefficients of the feed-back branch and of the

branch between the summing junction and the unit delay of integrator  $i$ . Equation (3) was derived using a small perturbation analysis and has been used for the predicted noise floor (horizontal straight line) of Fig. 4.

While in the modulator topology of Fig. 3 the loop filter deals only with quantization noise, the input branches connecting the input signal to the two summing junctions operate only on the input signal itself. Any error introduced at the summing junction in front of the quantizer is attenuated by the gain of the loop filter, and can be neglected (it causes the small self-image of Fig.4). On the other hand, any error introduced at the input summing junction appears unattenuated at the output of the modulator. It can be shown that with a complex input

signal of the form  $Ae^{j\varphi} e^{j2\pi\left(\frac{F_s}{4} + \Delta f\right)t}$ , a disturbance signal  $\delta_{in} Ae^{-j\varphi} e^{j2\pi\left(\frac{F_s}{4} - \Delta f\right)t}$  is introduced when applying the DEM scheme of Fig.1b), where  $\delta_{in}$  is the mismatch coefficient of the input branch. This is a self-image of the signal attenuated by  $\delta_{in}$ .

The feed-back DACs process both signal and quantization noise. Considering first the quantization noise, since the DACs process shaped quantization noise, the DEM scheme is very effective and it renders the mismatch of the DACs harmless. On the other hand, the DACs gain mismatch coefficient  $\delta_{DAC}$  does contribute to the signal self-image component. Taking into account both the mismatch coefficient  $\delta_{in}$  of the input branch and the DACs gain mismatch coefficient  $\delta_{DAC}$ , the attenuation  $\alpha_S$  of the signal self-image is given by:

$$\alpha_S = \delta_{in} - \delta_{DAC} \quad (4)$$

For many applications, an attenuation of 25 dB is sufficient and this is easily achieved. Furthermore, equation (4) suggests that the self-image component can be completely eliminated when  $\delta_{in}$  is equal to  $\delta_{DAC}$ . This is possible in SC implementation, by using the same capacitors for sampling the input and the DAC reference, which is also advantageous in term of kT/C noise.

### 3. EXTENSION TO MULTIBIT QUANTIZER

Though the topology of Fig. 3 can be implemented with single bit quantizers, it is desirable to use multibit quantizers in order to reduce the dynamic range requirements of the loop filter. Unfortunately, using a multibit quantizer poses stringent linearity specifications

on the feed-back DACs. For low-pass (LP)  $\Sigma\Delta$  modulators, this is normally addressed with mismatch noise shaping techniques [3]. In practice, a noise shaping scheme is implemented adding an Element Selection Logic (ESL) block in front of the DAC [3]. The ESL selects the DAC elements in such a way that the energy of the mismatch noise is moved away from the signal bandwidth.

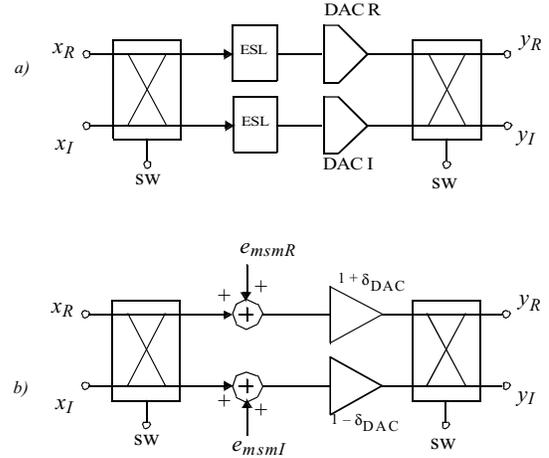


Fig.5: complex DAC (a) and its model (b).

Let's consider the pair of real DACs, DAC R and DAC I, which together constitute the complex feed-back DAC of the modulator of Fig. 3. Assume also that DAC R is made up of  $N$  1 bit DACs each of weight  $w_{Ri}$  and DAC I is made up of  $N$  1 bit DACs of weight  $w_{Ii}$ . Ideally,  $w_{Ri} = w_{Ii} = w_{av}$  for all  $i$ . In practice this is not the case. Let's define  $w_{av}$  as the average of the weights  $w_{Ri}$  and  $w_{Ii}$ . The DAC gain mismatch coefficient  $\delta_{DAC}$  is then given by:

$$\delta_{DAC} = -1 + \sum_{i=1}^N \frac{w_{Ri}}{Nw_{av}} = 1 - \sum_{i=1}^N \frac{w_{Ii}}{Nw_{av}} \quad (5)$$

The mismatch errors  $\epsilon_{Ri}$  of each DAC R element and the mismatch errors  $\epsilon_{Ii}$  of each DAC I are defined as:

$$\begin{aligned} \epsilon_{Ri} &= \frac{w_{Ri}}{1 + \delta_{DAC}} - w_{av} \\ \epsilon_{Ii} &= \frac{w_{Ii}}{1 - \delta_{DAC}} - w_{av} \end{aligned} \quad (6)$$

Notice that from the above definition it follows that

$$\sum_{i=1}^N \epsilon_{Ri} = \sum_{i=1}^N \epsilon_{Ii} = 0 \quad (7)$$

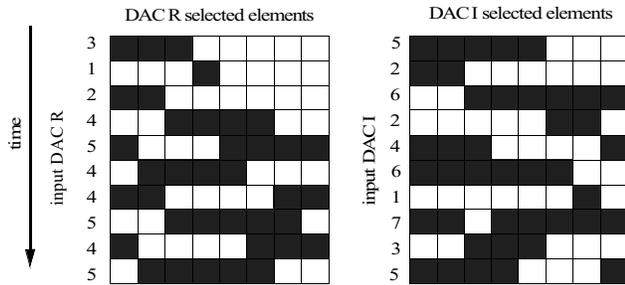


Fig. 6: element selection pattern.

For every clock cycle  $n$ , DAC R introduces an error  $e_{msmR}(n)$ , which is given by the sum of the  $\mathcal{E}_{Ri}$  of the elements selected to produce its output. Similarly, DAC I introduces an error  $e_{msmI}(n)$  which is given by the sum of the  $\mathcal{E}_{Ii}$  of the elements selected to produce its output.

From the above discussion it follows that the ESL and the DACs can be modelled as in fig. 5b). It can be shown that the power spectral density of mismatch noise  $e(n)$  at the output of the DAC of Fig. 5 is 0 at  $Fs/4$  if for some constant  $K$  and for any integer  $M$  [3]:

$$\left| \sum_{n=0}^M e(n) e^{-j\frac{\pi}{2}n} \right| < K \quad (8)$$

An example of a suitable selection pattern which satisfies (8) is shown in Fig. 6. The darkened elements are the ones selected to generate the current output. It can be observed that for DAC R, the elements of row 1,2,5,6,9,10 and so on are selected sequentially in a rotational fashion where the first unit element follows the last one. Also the elements of DAC R corresponding to row 3,4,7,8 and so on are selected sequentially in a rotational fashion, though following an independent sequence. Similarly, by analysing the selection pattern of the DAC I elements it can be concluded that these too are selected in a rotational fashion according to two independent sequences. However, now the elements corresponding to row 1,4,5,8,9 and so on belong to a first rotational sequence, and the elements corresponding to rows 2,3,6,7 and so on belong to the second rotational sequence. This scheme is essentially an extension to the complex case of the data weighted averaging technique and results in a first order shaping of the quantization noise.

#### 4. SIMULATION RESULTS

The 2<sup>nd</sup> order  $\Sigma\Delta$  complex modulator of Fig.3 with 3 bit quantizers employing the mismatch noise shaping selection scheme previously described in section 3 has been simulated with Simulink.

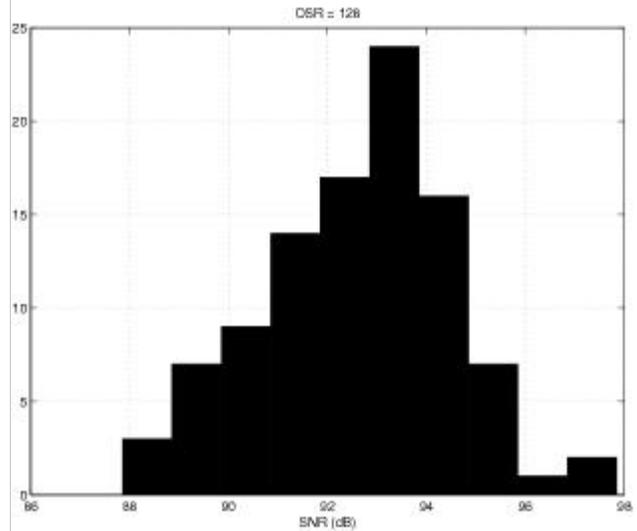


Fig.7: SNR histogram.

Fig. 7 shows an SNR histogram for 100 Monte Carlo simulations, where all the mismatch coefficients and the mismatch errors in the unit elements of the feed-back DACs are normally distributed with a standard deviation of 1%. The input is set to 80% of the full scale of the quantizers. Although this is far worse than a 1% matching, Fig. 7 shows that for an oversampling ratio (OSR) of 128 an SNR in excess of 88dB can be achieved for all the samples. A CMOS implementation of the ideas in this paper is in preparation and will be reported elsewhere.

#### 5. CONCLUSION

A new topology for multibit quadrature BP  $\Sigma\Delta$  modulators which is robust against mismatch has been introduced and validated with behavioral simulations.

#### 6. REFERENCES

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