A CMOS Low-Distortion Fully Differential Power Amplifier with Double Nested Miller Compensation

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Abstract—**A four-stage fully differential power amplifier using a double nested Miller compensated structure is presented. The multiple-loop configuration used results in a lower harmonic distortion, at least in the audio band, compared to conventional three-stage amplifiers with nested Miller compensation. Design criteria and conditions for good stability of amplifiers using a multiple- (greater than two) loop topology are presented. The amplifier operates with a single power supply which has a minimum value of 3 V. With a 5-V supply, power dissipation is 10 mW and THD is –83 dB for a 6-V_{p-p} differential output signal at 10 kHz and a load of 50 Ω. With 8-Ω load and for a 10-kHz, 4-V_{p-p} output signal, THD is -68 dB. The chip area is 0.625 mm^2 in a 1.5-μm single-poly, double-metal, n-well CMOS technology**

I. Introduction

In recent years many new very complex systems have been integrated into silicon chips. This has become possible especially through the use of new digital circuits with a continually increasing flexibility and precision. In this process many analog circuits have been substituted with digital ones. Although this tendency will continue, some analog blocks, especially those interfacing with the external world, cannot be replaced. One example is given by the power amplifiers or output buffers. Furthermore, as the precision and accuracy of DSP-based systems increase, the level of performance required from the analog interface circuits also increases.

In ISDN voice terminal equipment and digital telephone sets, for instance, there is the necessity to drive loads of 50–100 Ω and more than 100 nF for acoustic transducers, using CMOS technologies and a 5-V power supply [1]. Similar needs are present in battery-operated systems such as portable hi-fi systems and cellular and cordless phones, where sometimes power supply can be as low as 3 V. In all these cases general requirements are low distortion together with small die size and low quiescent current. However, it is difficult to satisfy all these requirements, especially regarding distortion, using previous design methodologies. In fact, for a buffer amplifier driving heavy loads, there is a trade-off between linearity on the one hand and power consumption and silicon area on the other. For instance, to improve open loop linearity while giving output currents of up to hundreds of milliamperes, very large widths (up to 10 000 μm) are used for the output devices resulting in large silicon area. Conversely, to improve closed loop linearity, a large unity-gain bandwidth and consequently a large power dissipation are required.

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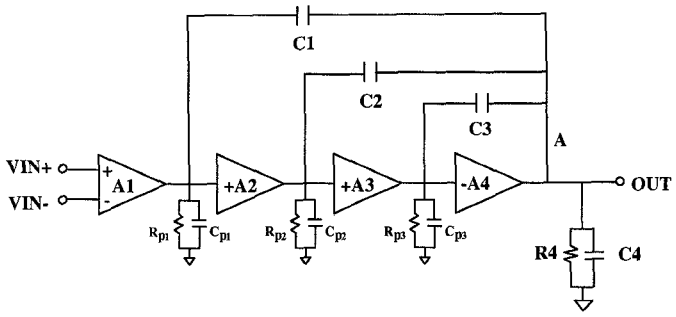

Fig. 1. Multiple-loop feedback topology.

Most recently reported buffer amplifiers [2]–[7] use a three-stage nested Miller compensated topology to get better linearity for a given power consumption and/or silicon area as compared with a simple two-stage Miller structure [8]. This paper goes a step further, presenting a differential power amplifier with four stages of gain (including the class AB output stage) with a double nested Miller compensation. This has resulted in a better linearity with lower power dissipation and smaller area even compared with a nested Miller topology.

In Section II of this paper, the multiple-loop compensation technique is presented and analyzed. Special attention is given to the key problem of stability. This is a particularly critical aspect of the design when using four or more stages and thus some basic principles for good stability are provided. The reasons why distortion is improved, at least in the audio band, are explained in Section III.

In Section IV the new amplifier topology is described, while experimental results are reported in Section V.

II. Stability in Multiple-Loop Amplifiers

The block diagram of a multiple nested Miller compensated amplifier is shown in Fig. 1. The case of a single-ended structure with four stages of gain is represented. The first stage is a differential input stage, the second and third ones are intermediate noninverting gain stages, and the last one is the inverting output stage delivering the power to the load represented by resistor R_4 and capacitor C_4. If a differential structure were used it would not be mandatory to use noninverting intermediate gain stages, but in this case a crossing of the intermediate compensation capacitors would be necessary to obtain a stable structure.

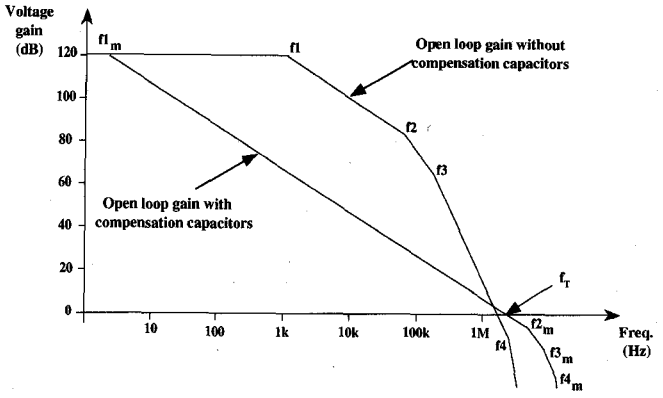

Fig. 2. Bode plot of an amplifier with double nested Miller compensation.

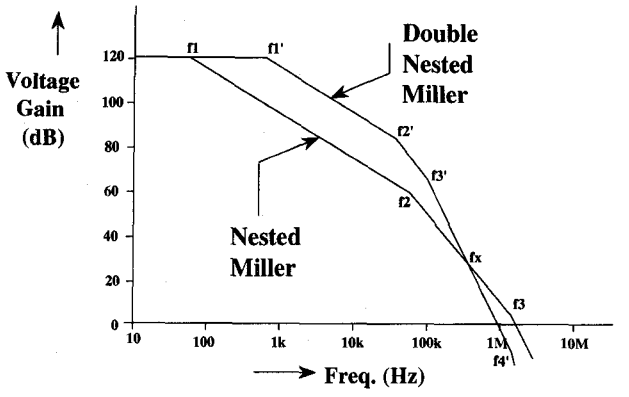

Fig. 3. Loop gains for a nested Miller and a double nested Miller compensated amplifier with compensation loops open.

A Bode plot for the amplifier is presented in Fig. 2. The poles of the open-loop frequency response without compensation capacitors are at frequencies

$$f_i = \frac{1}{2\pi R_{pi} C_{pi}}, \quad i = 1, 3$$
$$f_4 = \frac{1}{2\pi R_4 C_4} \tag{1}$$

where R_{pi} and C_{pi} are the parasitic output resistances and capacitances, respectively, of the ith stage, while R_4 and C_4 represent the external loads.

Consider now the movement of the poles when the compensation loops are closed. The insertion of the compensation capacitors C_i produces a "pole-splitting" effect similar to that occurring in a simple Miller compensated structure where the pole f_{1m} associated with the output of the first stage is moved to low frequency while the output pole is moved to high frequency [8]. In this case f_{1m} is pushed to very low frequency while all the other poles, included the one at the output, are pushed to high frequency. The position of the dominant pole f_{1m} is given by the following expression:

$$f_{1m} = \frac{1}{2\pi\, G_{m2}\, R_{p2}\, G_{m3}\, R_{p3}\, G_{m4}\, R_4 R_{p1}\, C_1} \tag{2}$$

which shows that f_{1m} is moved down in frequency by a factor equal to the product of the gains of all the following stages. In order to obtain a good phase margin, this pole must be at a very low frequency while the nondominant poles $f_{2m} \cdots f_{Nm}$ must be at frequencies higher than the unity-gain frequency f_T of the amplifier:

$$f_{im} > f_T \gg f_{1m}, \qquad i = 2, N \tag{3}$$

The exact position of the nondominant poles can be quite complex to calculate. In fact, if no special precaution is taken, these poles tend to interact with each other giving rise to complex pairs. This produces bumps in the frequency response, which is an indication of a critical design from the point of view of stability. A stable and robust design and a simple expression for the nondominant poles can, however, be obtained if the following rules are implemented:

$$\frac{G_{mi}}{C_i} \leq \frac{1}{2}\frac{G_{m\,i+1}}{C_{i+1}} \tag{4}$$

$$G_{mN} \gg G_{mi}, \qquad i = 1, N-1. \tag{5}$$

where G_{mi} is the transconductance of the ith stage. When the above rules are satisfied, the approximate position of the nondominant poles is given by the following expression:

$$f_{im} \sim \frac{G_{mi}}{2\pi\, C_i} \qquad i = 2, 4 \tag{6}$$

while the unity-gain frequency of the amplifier is given by

$$f_T \sim \frac{G_{m1}}{2\pi\, C_1}. \tag{7}$$

The first stability condition (equation (4)) requires each nondominant pole to be positioned at a frequency which is at least twice as high as that of the previous one. When this condition is satisfied, all the poles are sufficiently separated so as not to interact with each other, i.e. they are on the real axes according to (6). In this case each one of them can be associated with the output of each amplifying stage when computing the amplifier open-loop transfer function. The output of the first stage is associated with the dominant pole and the outputs of the following $n-1$ stages with the nondominant ones.

Equation (5) is always satisfied in the case of power operational amplifiers since the transconductance of the last stage must be very high, compared to that of the preceding stages, in order to drive heavy loads.

On the contrary, condition (4) is a pretty stringent one and tends to limit considerably the overall bandwidth of the amplifier as the number of stages is increased. Nonetheless, a lower distortion can be still obtained as explained hereafter.

It would be possible to overcome the bandwidth reduction effect using the technique called "multipath nested Miller compensation," which was recently presented for a three-stage amplifier [9]. In this amplifier an independent path was introduced to bypass the intermediate stage at high frequencies, forcing the amplifier to behave as a two-stage amplifier.

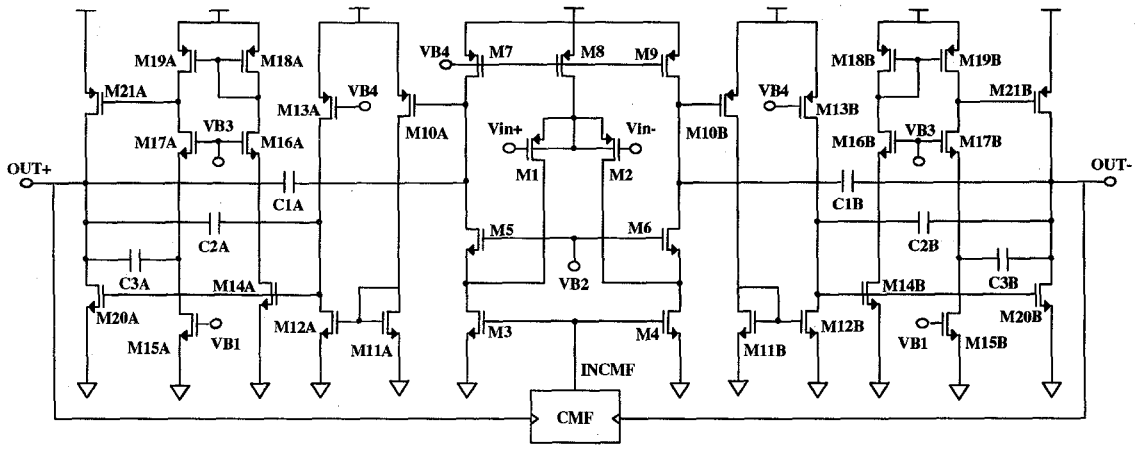

Fig. 4. Overall amplifier schematic.

From (3)–(7) it follows that the amplifier has a very good degree of stability even in the unity-gain closed-loop configuration.

III. Distortion in Multiple-Loop Amplifiers

In power amplifiers driving heavy loads and without problems of current driving (such as slew rate or output voltage clipping due to limited output current capability), distortion is mainly due to the output transistors. In fact, to get the required current driving capability without excessively large devices, the gates of the output transistors must be driven with a rail-to-rail voltage swing. As a consequence, these devices move from saturation to deep linear operation during each cycle of the output signal (a sinusoidal driving is assumed). The most critical situation for a given value of the impedance load is when the load is purely resistive. In fact, in this case there is a 180° phase shift between gate and drain voltages of the output devices so that the maximum peak of current in the load is required when the output voltage is at its maximum value and the gate voltage is at its minimum value. In this condition the output transistor may leave the saturation region during part of the output swing and, as a consequence, the gain of the amplifier is strongly reduced. This condition can be modeled with a large distortion source located in parallel with the output transistors.

When feedback loops are closed, distortion is reduced by a factor equal to the products of the gains of all the loops surrounding the distortion source (both external feedback and internal compensation loops). In a multiple-loop feedback configuration like that of Fig. 1, it can be shown that the linearization factor for the distortion coming from the output transistor can be computed by opening all the compensation loops and computing the gain of the structure obtained in this way. This can be accomplished by cutting all the connections between the compensation capacitors and the op-amp output (that is, cutting at point A in Fig. 1). To preserve the loads on all internal nodes after the loops have been opened, the compensation capacitors must be connected to ground.

Fig. 3 shows the loop gain for a nested Miller and a double nested Miller compensated amplifier with compensation loops open. The figure assumes that the two amplifiers are designed to give the same dc gain. To achieve this, a lower gain is used in the input stage of the double nested amplifier compared with the nested one. Thus the pole of the input stage in the double nested case is pushed to a higher frequency (f_1') thanks to a lower output resistance. The pole associated with the extra gain stage is located in the proximity of that associated with the second stage of the nested Miller circuit ($f_2' \sim f_2$). From Fig. 3 it can be seen that the double nested configuration has a larger loop gain (i.e., linearization factor) up to several hundred kilohertz (frequency f_x in the figure), even though the nested Miller configuration has a larger bandwidth. For the example of Fig. 3, the improvement between 1 and 20 kHz is about 20 dB. If the signal band is within this range, a 20-dB better closed-loop linearity can be expected for the double nested amplifier assuming the same open-loop nonlinearity. Note that at 100 kHz there is still an improvement when using a double nested configuration.

IV. New Amplifier Topology

The circuit schematic of the new four-stage amplifier is shown in Fig. 4. Because of the symmetry of the circuit only the left half section is analyzed. The input stage ($M1$–$M9$) is a folded gain stage. Input devices are p-channel to lower flicker noise. Their g_m is not very high so that the compensation capacitors resulting from (7) have a reasonable value for the given bandwidth. This also produces a good slew rate behavior even if the bias current of the input transistors is quite small ($12.5\,\mu$A).

The second stage is a noninverting gain stage composed of a common-source p-channel input ($M10A$), a current mirror ($M11A, M12A$), and a fixed current source ($M13A$) of $25\,\mu$A. The third stage ($M14A$–$M19A$) is similar to the previous one but of the complementary type. $M15A$ is a fixed current source of $50\,\mu$A. The output stage ($M20A$, $M21A$) uses a class AB topology with the p-channel transistor driven by the output of the third stage and the n-channel by the output of the second one. Note that the amplifier has a four-stage topology only from the input to the p-channel output transistor, while from the input to the output n-channel it has a three-stage topology. The gain difference from the input to the gate

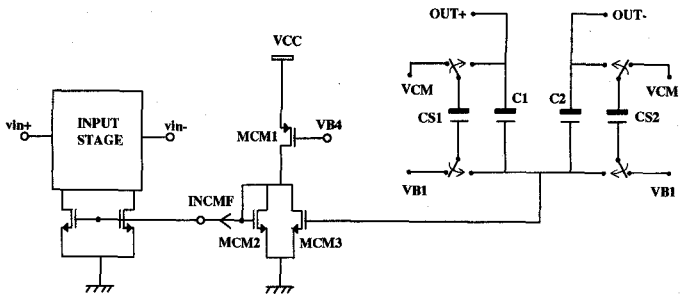

Fig. 5. Common-mode feedback circuit.

of these two output transistors is partially compensated by the larger g_m of the n-channel output device.

This configuration gives a tight control on the value of the quiescent current in the output transistors whose nominal value is 750 μA. The standard deviation of this current over all possible process variations was measured to be only 8%. In fact, the main source of fluctuations of the quiescent current is the mismatch in the current ratio between $M14A$ and $M20A$ that is quite small.

There are two compensating capacitors ($C1A$ and $C2A$) from the amplifier output to the outputs of the first and second stage. A third compensation capacitor ($C3A$) is inserted from the amplifier output to the source of the common-gate n-channel device ($M17A$) placed at the output of the third stage. Therefore, the two more external nested compensation loops are of the Miller type, while the internal one realizes a cascode-type compensation [10]. The output pole of the amplifier resulting from the insertion of the compensation capacitor $C3A$ is at a higher frequency than that which would result from a normal Miller loop. In fact, the frequency of this pole is approximately

$$f_{4m} = \frac{G_{m4}}{2\pi\,(C_L + C3A)}\,\frac{C3A}{C_{p3}} \tag{8}$$

where G_{m4} is the transconductance of the p-channel output transistor and C_{p3} is the parasitic capacitance at its gate. Thus, f_{4m} is increased by a factor equal to $C3A/C_{p3}$ with respect to a normal Miller loop. This helps to increase overall stability in the presence of a capacitive load. Using this approach the output pole is moved to a higher frequency leaving more space between itself and the unity-gain frequency to place the other two high-frequency poles resulting from the insertion of $C1A$ and $C2A$. Also the amplifier's power supply rejection is improved in this way [10]. The maximum increase in the frequency of this output pole is limited by the parasitic pole at the source of $M17A$ which is located at the frequency $G_{mM17A}/2\pi(C_{3A} + C_{gsM17A})$. Trying to further increase the frequency of the output pole results in complex poles giving a peaking in the frequency response.

A dynamic common-mode feedback has been used as shown in Fig. 5 [11]. A voltage related to the average value of the outputs is taken through a switched-capacitor network and is applied to an inverting stage in order to have the right polarity for the common-mode correction signal at node $INCMF$. In this way the common-mode feedback loop has the same poles as the differential loop plus the pole

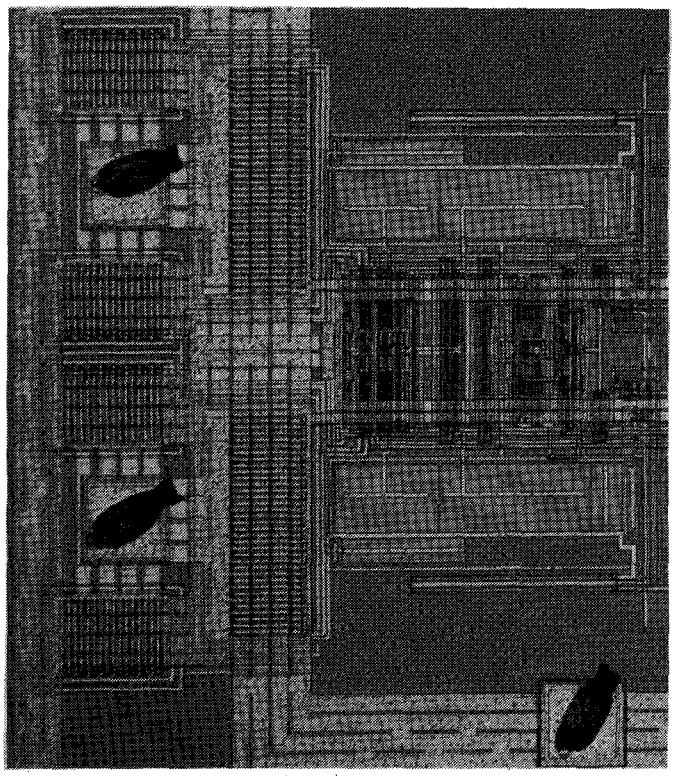

Fig. 6. Chip microphotograph.

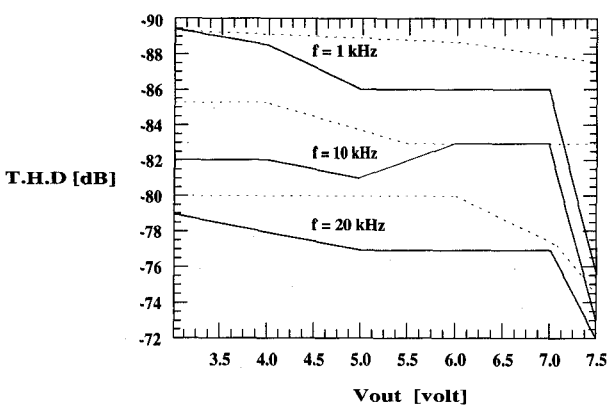

Fig. 7. Measured THD versus output swing with 50 Ω (—) and 100 Ω (···) load at various frequencies.

associated with the node $INCMF$. This extra pole, however, is at a much higher frequency than the unity-gain frequency. Thus, a similar bandwidth for both the main amplifier and the common-mode amplifier can be obtained. This type of common-mode feedback is highly linear so that there is no distortion degradation due to its presence. Moreover, it does not increase power dissipation.

The device sizes for the amplifier are reported in Table I.

V. Experimental Results

A microphotograph of the differential amplifier is shown in Fig. 6. The amplifier is implemented in a 1.5-μm CMOS n-well double-metal, single-poly technology with implanted capacitors (poly/n$^+$). The overall active area is 0.625 mm^2.

Fig. 7 shows the measured total harmonic distortion versus output swing with loads of 50 and 100 Ω and a power supply

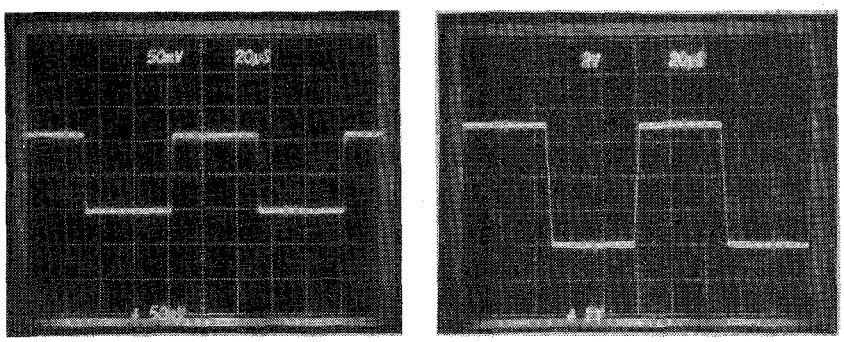

Fig. 8. Amplifier step response.

TABLE I
COMPONENT SIZES

M1 = M2	500/5	M17A = M17B	300/2
M3 = M4	100/8	M18A = M18B	50/2.5
M5 = M6	150/2	M19A = M19B	50/2.5
M7 = M9	100/6	M20A = M20B	3000/1.5
M8	200/6	M21A = M21B	3500/1.5
M10A = M10B	100/4	C1A = C1B	17.5 pF
M11A = M11B	50/2.5	C2A = C2B	5 pF
M12A = M12B	50/2.5	C3A = C3B	12 pF
M13A = M13B	200/6	MCM1	200/6
M14A = M14B	200/1.5	MCM2 = MCM3	50/8
M15A = M15B	200/8	C1 = C2	3.6 pF
M16A = M16B	300/2	CS1 = CS2	1.2 pF

TABLE II
AMPLIFIER PERFORMANCE SUMMARY

VDD = 5V @ T = 25 °C @ Vout / Vin = 1 1.5 - μm CMOS double metal, single polysilicon	
Quiescent Power Dissipation	10 mW
Unity Gain Bandwidth	2 MHz
Slew Rate	1.5 V / μsec
Output Noise (Audio Band-Pass)	10 μV
Area	0.625 mm^2
Total Harmonic Distortion	
Vout = 7 Vpp, f= 1 KHz, R_L = 50Ω	-86 dB
Power Supply Rejection	
f= 1 KHz	> 90 dB
f= 100 KHz	71 dB

of 5 V at three different frequencies (1, 10, and 20 kHz). In the audio band, distortion at 6 V_{p-p} is always lower than −77 dB for 50 Ω and -80 dB for 100 Ω. There is no significant linearity degradation up to a voltage swing of 7 V_{p-p}. This limit could be increased even more enlarging the output transistors. No degradation in linearity for small input levels due to crossover distortion has been detected.

In the previous measurements and in all the following ones an inverting configuration with unity gain is assumed and the capacitive load is intended to be 250 pF. However, the behavior of the circuit remains unchanged for capacitive loads from 0 to 1 nF.

Fig. 8 shows the step responses of the amplifier in unity-gain configuration in case of a large step of 7 V_{p-p} and a small one of 100 mV_{p-p} with a load of 50 Ω and 200 pF. The response is quite clean demonstrating that a good stability is achieved.

PSR is always better than 72 dB up to 90 kHz.

There is no significant variation in the obtained results if a 3-V power supply is used and a reduced output swing of 2 V_{p-p} is considered. This swing could be increased simply enlarging the output transistors.

The main amplifier performances are summarized in Table II.

VI. CONCLUSIONS

A fully differential power amplifier with four stages of gain was presented. The double nested Miller compensation approach used leads to very low distortion. The reported circuit operates from a single power supply with a minimum value of 3 V (in this case the input and output voltages must be properly scaled).

The amplifier is stable for a wide range of loads, both capacitive and/or resistive. This design demonstrates that robust amplifiers can be designed with a number of stages in excess of three. Stable operation can be achieved with a small reduction in bandwidth, which nevertheless produces a large linearity improvement in the audio band and beyond.

In the audio band measured distortion is about 20 dB smaller than that of a similar amplifier with one less gain stage and using a simple nested Miller compensation (obtained suppressing the first intermediate gain stage). This confirms experimentally how, starting from the same sources of distortion, the amplifier topology can drastically change the closed-loop linearity.

Furthermore, simulations show that in some cases (e.g., if only the telephone band is important) going to an even higher number of stages (e.g., 5) can further improve linearity. Alternatively, the same distortion can be achieved with smaller power consumption. This opens new possible solutions for power amplifier design.

ACKNOWLEDGMENT

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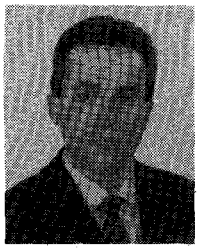

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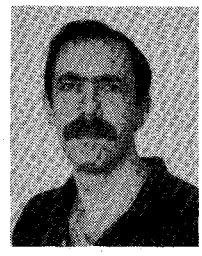

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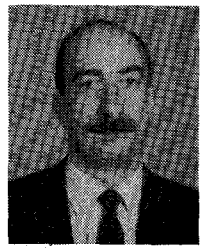

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