A Low-Power, High-Speed, Current-Feedback Op-Amp with a Novel Class AB High Current Output Stage

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***Abstract*— A complementary bipolar low-power, high-speed, current-feedback operational amplifier is described. The amplifier incorporates a new Class AB output stage that enables high output current drive of 100 mA and large voltage swing within 1 V of the supply rails while operating at low quiescent current of 1.5 mA. The amplifier was fabricated in a junction-isolated complementary bipolar process with NPN/PNP f_t of 4.5/3.8 GHz. The amplifier, configured for noninverting gain of two and 100-Ω load, provides 3-dB bandwidth of 110 MHz and 2-V pulse rise time of 7 ns.**

***Index Terms*—Analog integrated circuits, bipolar analog integrated circuits, operational amplifiers.**

I. Introduction

An increasing number of video and communication applications require line or cable driver circuits that can provide high peak output current with large bandwidth and low distortion while operating on low quiescent current and low supply voltage of +5 V or ±5 V. This requirement is well served by complementary bipolar amplifier circuits. An excellent review of modern complementary bipolar high-speed monolithic operational amplifiers, including current-feedback op-amps, is given in [1]. A simplified circuit schematic of a typical modern complementary bipolar high-speed current-feedback op-amp is shown in Fig. 1. The basic elements of the architecture are unity gain input buffer, current mirror gain stage, and unity gain output buffer. Complementary emitter followers Q1–Q4 form the input buffer. The collector signal currents of transistors Q3 and Q4 are turned around and summed through Wilson current mirrors formed by Q5–Q7 and Q8–Q10, respectively. This signal current injected into the high impedance node sets the open-loop gain of the amplifier. The output buffer (Q13–Q16) provides near unity voltage gain and isolates the high impedance current summing node from the amplifier load. The single gain stage architecture provides high bandwidth at the expense of open-loop transimpedance. The loss of dc accuracy is usually acceptable in the high-speed applications in which these amplifiers are employed.

Nearly all monolithic complementary bipolar high-speed current-feedback op-amps are a variation of the architecture just described, with variations and additions to meet design goals and accommodate the characteristics of the fabrication process. An overview of the design goals for the present op-amp design are given here to establish the motivation for the new output stage design that is the innovative feature of the op-amp design described in this paper. An increasing number of applications for high-speed op-amps require operation from a single +5-V supply, while a significant number still utilize bipolar ±5-V supplies, making operation over a range of supply voltages a desirable design goal. Typical applications require output voltage swing of at least ±1 V, making output swing to within 1 V of the power supply rails a design goal. In line-driving applications, where the load impedance is relatively low, high output current capability is required. For example, 2 V into 25 Ω requires 80 mA output current. Thus, output current capability of ±100 mA was established as a design goal. Although high output current capability may be required, low quiescent current is often required to keep system power consumption as low as possible. This combination of high output current capability and low quiescent current is particularly advantageous in systems with a low duty cycle or high peak-to-average output current ratio. For op-amps in the 100-MHz bandwidth class, supply current in the 1–3 mA range represents a good tradeoff between performance and quiescent power dissipation. In order to serve a wide range of high-speed applications, 3-dB bandwidth greater than 100 MHz, and slew rate greater than 250 V/μs were established as speed goals. A final design goal was to implement the design in a mature, low-cost complementary bipolar technology with small die size, keeping cost low and allowing packaging in a tiny surface outline transistor (SOT) package.

In this paper, a current-feedback op-amp is described which incorporates a new output stage to overcome the limitations of emitter follower output stages in meeting the design criteria described above. In Section II, limitations of typical emit-

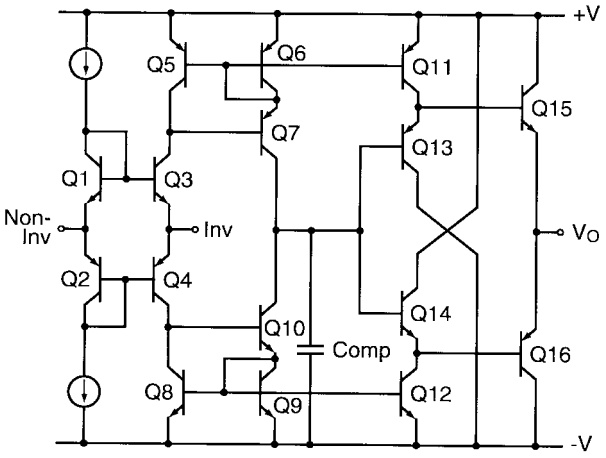

Fig. 1. Simplified circuit schematic of a typical high-speed complementary bipolar current-feedback op-amp.

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ter follower output stages are discussed. Circuit operation of a new output stage which overcomes these limitations is described in Section III. In Section IV, the design of a complete current-feedback op-amp incorporating the new output stage is described. Amplifier measurement results are presented in Section V, followed by conclusions given in Section VI.

II. Limitations of Emitter Follower Output Stage

A circuit schematic of the four-transistor Class AB emitter follower is shown in Fig. 2(a). This circuit configuration is sometimes referred to as a double buffer since it is effectively a cascade of two emitter follower stages. The linear output voltage range of this circuit is approximately

$$V_O^+ \approx V_{\rm CC} - [V_{\rm BE} + V_{\rm SAT}] \approx V_{\rm CC} - 1\ {\rm V} \quad (1)$$

$$V_O^- \approx V_{\rm EE} + [V_{\rm BE} + V_{\rm SAT}] \approx V_{\rm EE} + 1\ {\rm V} \quad (2)$$

assuming that the voltage compliance of current sources $I1$ and $I2$ is approximately the saturation voltage of a single transistor. Output current capability of this circuit is approximately

$$I_O^+ \approx I_1 \cdot \beta_{\rm Q3} \approx I_1 \cdot \beta_{\rm NPN} \quad (3)$$

$$I_O^- \approx I_2 \cdot \beta_{\rm Q4} \approx I_2 \cdot \beta_{\rm PNP}. \quad (4)$$

This limitation can be troublesome for high-speed complementary bipolar processes where $\beta_{\rm PNP}$ can be 20 or even lower, especially at cold operating temperatures. Output current capability is often improved by adding an additional emitter follower stage, resulting in the triple-buffer circuit shown in Fig. 2(b). The linear output voltage range of this circuit is approximately

$$V_O^+ \approx V_{\rm CC} - [2 \cdot V_{\rm BE} + V_{\rm SAT}] \approx V_{\rm CC} - 2\ {\rm V} \quad (5)$$

$$V_O^- \approx V_{\rm EE} + [2 \cdot V_{\rm BE} + V_{\rm SAT}] \approx V_{\rm EE} + 2\ {\rm V} \quad (6)$$

assuming that the voltage compliance of current sources $I1$ and $I2$ is approximately the saturation voltage of a single transistor. Output current capability of this circuit is approximately

$$I_O^+ \approx I_1 \cdot \beta_{\rm Q5} \cdot \beta_{\rm Q3} \approx I_1 \cdot \beta_{\rm NPN}^2 \quad (7)$$

$$I_O^- \approx I_2 \cdot \beta_{\rm Q6} \cdot \beta_{\rm Q4} \approx I_2 \cdot \beta_{\rm PNP}^2. \quad (8)$$

The emitter follower double buffer provides good output voltage swing range, but has poor output current capability relative to its quiescent current. The triple buffer provides good output current capability relative to quiescent current, but does not have adequate output voltage swing when operated on a single +5-V power supply. An output buffer that has both the large voltage swing characteristics of the double buffer and the large output current characteristics of the triple buffer is desired to meet the stated design objectives.

III. Output Stage Design

A circuit which offers the potential to simultaneously provide the desired voltage swing and large output current capability is shown in Fig. 3. The output of this circuit is the parallel combination of common emitter devices (Q5, Q6) and emitter follower devices (Q3, Q4). Current sources ($I3$, $I4$) source/sink the quiescent current of emitter follower devices (Q3, Q4). All of the signal current in the collectors of emitter follower devices (Q3, Q4) is available to drive the bases of common emitter output devices (Q5, Q6). This results in output current capability enhancement of the four-transistor buffer by a factor of $\beta_{(\rm Q5,Q6)}$. In practice, this circuit cannot be implemented directly because temperature and process variations in β and Early voltage result in wide variations in the quiescent current of common emitter output devices (Q5, Q6). A means for controlling the quiescent current of the common emitter output devices that does not limit the signal current gain is required.

A complementary common emitter output stage [2], [3] is shown in Fig. 4. The circuit was originally described as a

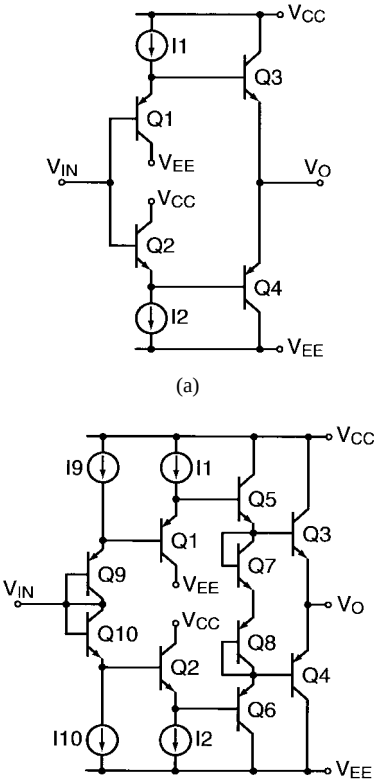


Fig. 2. Complementary bipolar emitter follower circuits: (a) double buffer and (b) triple buffer.

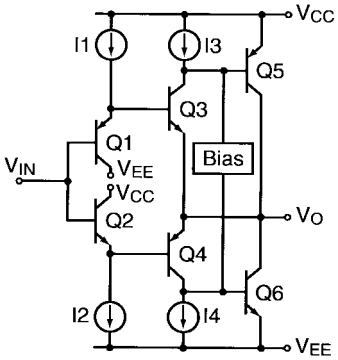


Fig. 3. Simplified circuit schematic of enhanced complementary emitter follower output stage.

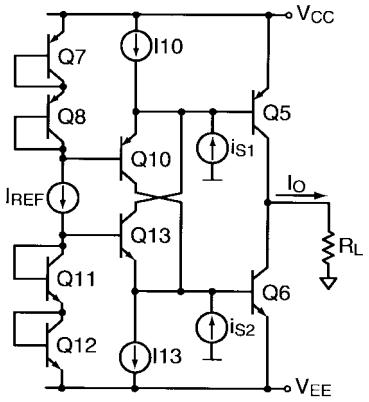


Fig. 4. Complementary common emitter output stage.

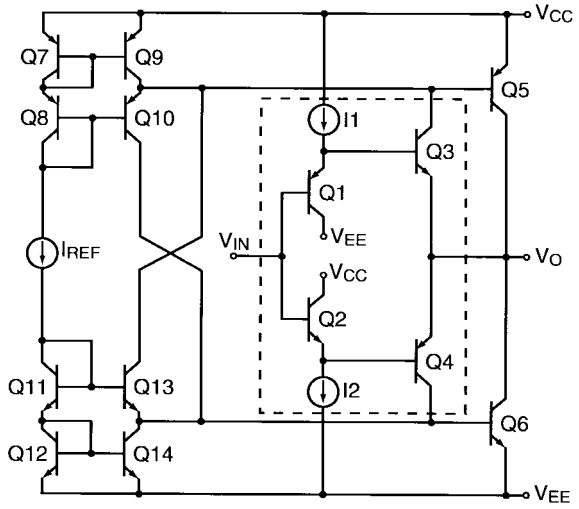


Fig. 5. Class AB high current output stage.

voltage gain stage in which an input signal voltage is applied at either the base of Q5 or the base of Q6. However, the circuit can also be operated with current inputs, and unlike voltage inputs, the signals can be applied at both inputs as shown in Fig. 4. The operating point is established by IREF, $I10$, $I13$, and the transistor area ratios. Current gain is approximately

$$I_O \approx -\beta_{Q5,Q6} \cdot [i_{S1} + i_{S2}]. \tag{9}$$

When the output current I_O is larger than the quiescent current of Q5 and Q6, the circuit operates as a Class AB circuit. That is, when output current is sourced, Q5 is the dominant active output device, while Q6 becomes the dominant active device as output current is sunk. Thus, current gain is approximately $-\beta_{Q6}$ for large positive input current and $-\beta_{Q5}$ for large negative input current. A practical implementation of the circuit shown in Fig. 3 is obtained if the collectors of a complementary emitter follower are connected at the current inputs of the circuit in Fig. 4. A simplified circuit schematic of the complete class AB high current output stage is shown in Fig. 5. A brief description of circuit operation follows.

Consider a positive going signal applied to the input at $V_{\rm IN}$ which results in sourcing output current to a load connected to V_O. As load current begins to flow, the current through Q3 increases while current through Q4 decreases. The increasing

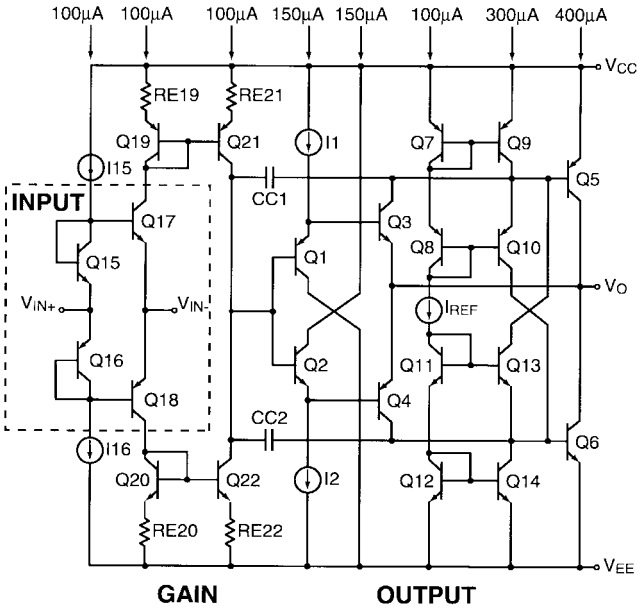


Fig. 6. Current-feedback op-amp simplified schematic.

current entering the collector of Q3 decreases the potential at the base of Q5, resulting in increased Q5 current which adds to the total current sourced to the load. The decreasing potential at the base of Q5 results in decreasing current in Q10. This reinforces the reduced current in Q4, resulting in lower potential at the base of common emitter output device Q6. The collector current in Q6 is reduced, further enhancing the net sourcing of current to the load. Note that the reduced potential at the base of Q6 also results in increased current in Q13, further reinforcing the net current sourcing action of the circuit. When the net-sourced load current is much greater than the common emitter output device Q5 quiescent current, the common emitter device Q5 provides a current gain of approximately $\beta_{\rm PNP}$ times the emitter follower Q3 output current. This also has the effect of reducing the output impedance of the emitter follower by a factor of approximately β. The circuit operates in a complementary fashion for negative input signals. The output stage can be viewed as a current-feedback amplifier configured for noninverting unity gain with a zero-ohm feedback resistor. The dominant pole, at the collectors of emitter follower devices Q3 and Q4, is due primarily to the input resistance and Miller-multiplied base-collector capacitance of the output common emitter devices Q5 and Q6. This closed-loop amplifier must be examined carefully to ensure sufficient phase margin. Since this circuit does not employ emitter degeneration, quiescent current can be somewhat variable due to device mismatches and finite device Early voltage.

IV. Current-Feedback OP-AMP Design

The Class AB high current output stage has been designed into a current-feedback op-amp. A simplified circuit schematic of the op-amp is shown in Fig. 6. The output stage is designed to be intrinsically stable without any additional compensation. The input stage is a complementary diode input emitter follower (Q15–Q18). The input emitter follower collec-

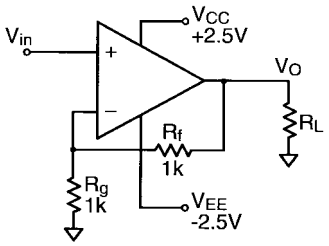


Fig. 7. Op-amp measurement configuration.

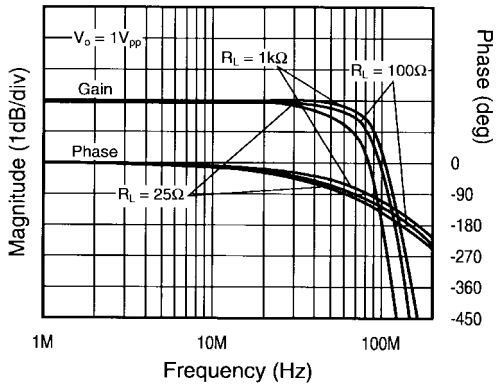


Fig. 8. Measured frequency response versus load resistance.

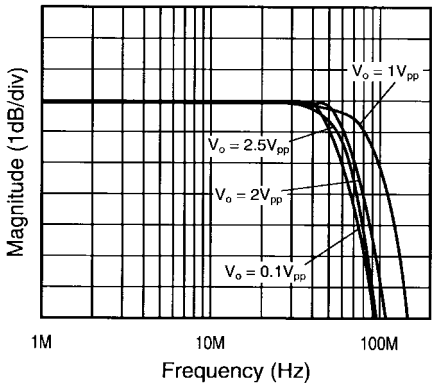


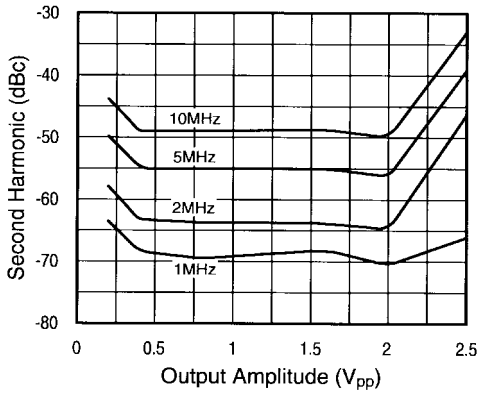
Fig. 9. Measured frequency response versus output amplitude.

tor currents drive complementary current mirrors (Q19–Q22, RE19–RE22), which provide current gain of approximately one. Emitter degeneration resistors are employed to improve the gain mirror accuracy and matching. The mirror outputs are connected directly to the input of the output stage. Compensation capacitors CC1 and CC2 establish a single dominant pole for the overall amplifier and are set to values which maximize bandwidth when the op-amp is configured for a voltage gain of $+2$ with a feedback resistor value of 1 kΩ.

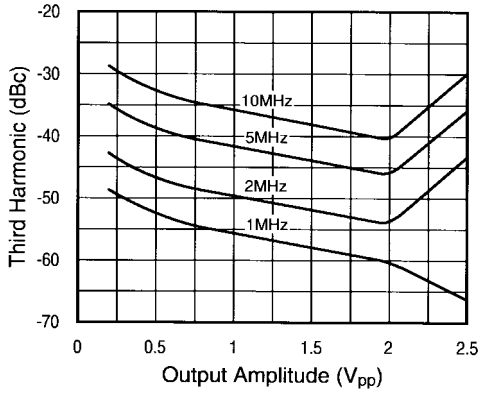
Nominal quiescent current of the amplifier is 1.5 mA. A temperature-compensated bias network and current mirrors provide the constant currents shown in the schematic. A 2-b metal fuse link trim is incorporated to achieve a tighter range of supply current over process variations. The circuit was designed for fabrication in CBIC-U2 [4], a mature junction-isolated complementary bipolar process with NPN/PNP f_t of 4.5/3.8 GHz. Die size is 0.8 mm^2, enabling packaging in a tiny 5-pin SOT package.

TABLE I
SUMMARY OF OP-AMP CHARACTERISTICS AND PERFORMANCE

Power Supply (V_{CC} -V_{EE})	5V to 10V
Supply Current	1.5 mA
Output Current	> ±100mA
Output Voltage (V_{CC}/V_{EE} = ±5V)	± 4.0V
Open Loop Transimpedance (DC)	320,000 Ω
3dB Bandwidth V_{CC}/V_{EE} = ±2.5V, V_{OUT}=1V_{PP} R_F=1K, A_V=+2, R_L=100	110 MHz
Rise/Fall Time V_{CC}/V_{EE} = ±2.5V, V_{OUT}=2V_{PP} R_F=1K, A_V=+2, R_L=100	7 nsec
Distortion f = 1MHz V_{CC}/V_{EE} = ±2.5V, V_{OUT}=2V_{PP} R_F=1K, A_V=+2, R_L=25	2nd -70 dBc 3rd -60 dBc
Technology	Lucent CBIC-U2 Junction-Isolated Complementary Bipolar
NPN / PNP f_t	4.5 / 3.8 GHz
Die Size	0.80 mm^2



(a)



(b)

Fig. 10. Measured distortion (a) second harmonic and (b) third harmonic.

V. MEASUREMENT RESULTS

Measurements of the current-feedback op-amp design confirm the operation and performance advantages of the novel output stage design. Characteristics of the amplifier are summarized in Table I. Many performance parameters meet or exceed those of similar designs in the same process that require

significantly higher quiescent current. All data presented here is for minimum power supply voltages of ± 2.5 V, with the amplifier configured as shown in Fig. 7. In general, improved performance is obtained at higher supply voltage, due to the reduced collector-substrate and collector-base capacitances.

The measured frequency response of the amplifier configured for noninverting gain of two is shown in Fig. 8. At an output level of 1.0 $V_{\rm pp}$, the 3-dB bandwidth is in excess of 100 MHz for loads greater than 100 Ω and is reduced to 90 MHz at a load of 25 Ω. Measured frequency response for several output levels when configured for a gain of two and driving a 100-Ω load is shown in Fig. 9. Bandwidth at very small output signal levels is somewhat reduced due to the very low quiescent current in the output common emitter devices, while bandwidth reduction at large output signal levels is due to the slew rate limitations of the amplifier.

Measured second and third harmonic distortion versus output level for a noninverting gain of two and load resistance of 25 Ω at several frequencies in the 1 to 10 MHz range is shown in Fig. 10. Second harmonic distortion, shown in Fig. 10(a), is relatively constant over a wide range of output levels. This is typical of a Class AB circuit in which second harmonic distortion is generated by mismatch between the two paths of the complementary circuit. Third harmonic distortion, shown in Fig. 10(b), improves with increasing output signal level up to about 2 $V_{\rm pp}$. This is also typical of Class AB circuits in which third-order distortion is generated by a nonlinear characteristic as the circuit crosses over the two paths of the complementary circuit. Distortion is reduced with increasing signal level because the crossover region is a smaller fraction of the overall signal. Distortion performance is a function of load impedance and improves significantly as load resistance is increased.

VI. Conclusion

A novel Class AB output stage that operates as an enhanced complementary four-transistor emitter follower has been developed. The circuit provides output voltage swing to within 1 V of the power supply rails and exceptional output current drive capability while operating at low quiescent current. The output stage enabled the design of a high-performance, low-power current-feedback operational amplifier implemented in a junction-isolated high-speed complementary bipolar process. The op-amp exhibits equivalent performance at much lower quiescent power compared to similar designs in the same fabrication process.

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