A THIRD-ORDER MULTIBIT SIGMA-DELTA MODULATOR WITH FEEDFORWARD SIGNAL PATH

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ABSTRACT

A third-order multibit sigma-delta modulator with feedforward path is described in this paper. This sigma-delta modulator operates at very low oversampling ratios and the in-band noise can be suppressed significantly to achieve a high resolution. The circuit's sensitivity to opamps nonlinearity is minimized through the use of the feedforward path. The simulation results for a 5-bit implementation show 102dB SFDR and 84.7dB peak SNDR over a 3MHz signal bandwidth, at OSR of 16.

I. INTRODUCTION

There is a great deal of interest in extending the bandwidth of sigma-delta Σ-Δ modulators for wideband applications. There are many ways to increase the bandwidth of a sigma-delta converter. Each method involves an alteration of one or more of the parameters available to the designer, that is the sampling frequency, the number of bits in the quantizer, the oversampling ratio and the modulator loop order. An alternative to increase the effective sampling frequency is to lower the OSR. There are several ways to do so. One solution is to improve the noise-shaping characteristic by employing higher-order modulators, [5]. Another alternative and perhaps the most practical approach, is to replace the single-bit quantizer by a multi-bit quantizer, [4]. This allows the OSR to be reduced without trading resolution to maintain stability. One approach to escape the DAC nonlinearity effects is to cascade a single-bit and a multi-bit modulator [5]. One new approach is to cascade multibit modulators, [1], [6], [9]. Combining Σ-Δ modulators with multibit quantization is an effective means to achieve a high dynamic range and a wide bandwidth. The major limitation in designing multibit sigma-delta modulators is that very good component matching is required for feedback DAC linearity. Good attenuation of feedback DAC noise due to component mismatches can be provided by different liniarization algorithms, which ideally can achieve a linear DAC.

The circuit presented here realizes the third-order noise shaping through a 5-bit 3rd order Σ-Δ modulator with feedforward path. The effect of opamp and DAC nonlinearities on the SNDR of this Σ-Δ modulator is analysed. It is shown that this topology is less sensitive to the nonlinearities of the opamps.

II. SYSTEM-LEVEL CONSIDERATIONS

Fig. 1 shows the block diagram of a traditional third order 5-bit Σ-Δ modulator. Fig. 2 shows the block diagram of the third order 5-bit Σ-Δ modulator that is proposed in this work. The noise-shaping filter is a third-order topology with a cascade of integrators in a single loop and a feedforward signal path. This topology differs from the previous third-order Σ-Δ modulators. The feedforward signal path concept [8] has been extended to third-order noise shaping to realize a reduced sensitivity to opamps nonlinearities and to relax the stability requirements.

In the traditional third-order Σ-Δ modulators the output is given by:

$$Y(z) = z^{-3} \cdot X(z) + (1 - z^{-1})^3 \cdot Q(z) \qquad (1)$$

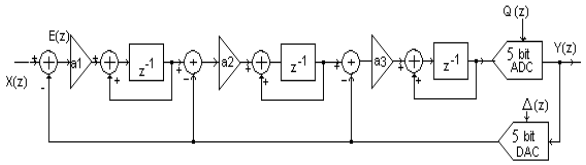


Figure 1. Block diagram of the traditional 3rd order 5-bit Σ-Δ modulator

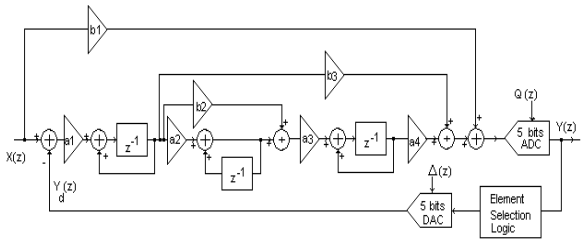


Figure 2. Block diagram of the 3rd order 5-bit Σ-Δ modulator with feedforward path

The signal transfer function is $STF(z) = z^{-3}$ and the noise transfer function is $NTF(z)=(1-z^{-1})^3$. In this case the harmonics of the input signal created due to the nonlinear opamps will appear at the modulator output shaped by third-order high-pass transfer function. In wideband applications, the attenuation provided by a 3rd order high-pass transfer function at a low oversampling ratio is not enough. One solution is to design low distortion opamps.

In the Σ-Δ modulator with feedforward path the nonlinearity problem is achieved by making the signal transfer function, STF(z) exactly equal to 1. The proposed topology combines the advantage of sigma-delta modulator with feedforward path and the multibit quantizer to achieve high dynamic range and wideband A/D conversion. This topology uses only one DAC in the feedback path. This advantage is very important for multibit quantizer because of this reduces the complexity of circuit and the chip area. Another advantage of this topology is that the integrators process quantization noise only and than their performance requirements are relaxed.

By applying linear analysis, the output of the third order Σ-Δ modulator with feedforward path is given by

$$Y(z) = STF(z) \cdot X(z) + NTF(z) \cdot Q(z) \qquad (2)$$

where the signal transfer function must be STF(z)=1, without changing the third-order noise transfer function, NTF(z).

The noise transfer function for the topology presented in Fig. 1 is:

$$NTF(z) = \frac{(1-z^{-1})^3}{D(z)} \qquad (3)$$

where for $b_1=1$, D(z) is

$$D(z) = 1 + (a_1 b_3 - 3) \cdot z^{-1} + \\ + \left[3 - 2a_1 b_3 + a_1 a_3 a_4 (a_2 + b_2)\right] \cdot z^{-2} \qquad (4) \\ + (a_1 b_3 - a_1 a_3 a_4 b_2 - 1) \cdot z^{-3}$$

The design of 3rd order multibit Σ-Δ modulator with feedforward path was done using the CLANS methodology [5], [7] and several MATLAB simulations [2]. The coefficients were chosen for generating the peak SNDR of the modulator and to guarantee that the baseband quantization noise is independent of the input signal. The final values for the coefficients are $a_1=1$, $a_2=0.7499$, $a_3=1$, $a_4=1$, $b_2=1.6374$, $b_3=2.6062$.

In this topology, all the zeros of the noise transfer function, NTF(z) are placed at z=1.

The three integrators in the forward path of the modulator are fully-differential SC integrators. The effect of the nonlinear opamp dc transfer characteristic on the distortion performance of the modulator has been considered. Therefore, in this analysis, nonlinear opamp dc transfer characteristic is given by a cubic function:

$$y = k_1 \cdot x + k_3 \cdot x^3 \qquad (5)$$

The 5-bit quantizer is a flash ADC architecture. The nonlinearity errors due to resistor mismatch, hysteresis and other such phenomenon can be represented as an additional error term added at the quantizer. Thus this nonlinearity error is 3rd order shaped just as the quantization noise from this quantizer is shaped.

The most important design consideration for realizing a high-order multibit Σ-Δ modulator is the feedback multibit DAC. In the third-order modulator shown in Fig. 1, using a 5-bit internal DAC increases the peak SNR. However, the multibit DAC nonlinearity degrades the SNR in real circuits. Due to element mismatch, the DAC will also add an error term to the signal output. Hence the output signal is given by

$$Y(z) = X(z) + NTF(z)Q(z) - \left[1 - NTF(z)\right]\Delta(z) \qquad (6)$$

where Δ(z) is the error inserted due to DAC nonlinearity.

Therefore, a 5-bit implementation using the mismatch shaping technique [5] in the internal DAC is an effective design strategy for high-speed and high-precision ADC. The 1st order mismatch shaping technique has been used in the feedback DAC.

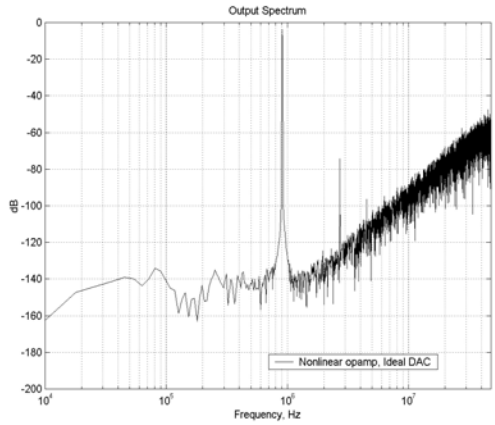
For the successful design of a third-order multibit Σ-Δ modulator with feedforward path, it is important to establish the sensitivity of the system's performance to major circuit nonidealities.

III. SIMULATION RESULTS

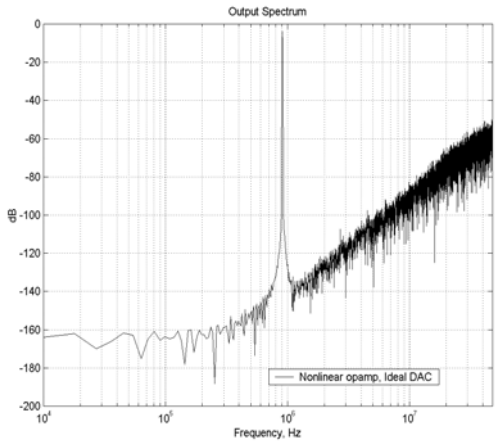
All simulations have been done using MATLAB and the Schreier Σ-Δ Modulators Toolbox. To take into account nonidealities, the major circuit effects that can introduce distortion are included in the models: finite opamp gain, gain error, opamp nonlinearity, and DAC mismatch. The fully differential SC integrator model uses an opamp with a 60dB dc gain and a transfer characteristic with cubic type nonlinearity.

The multibit quantizer is a flash A/D converter that consists of a resistive divider ladder followed by a bank of comparators.

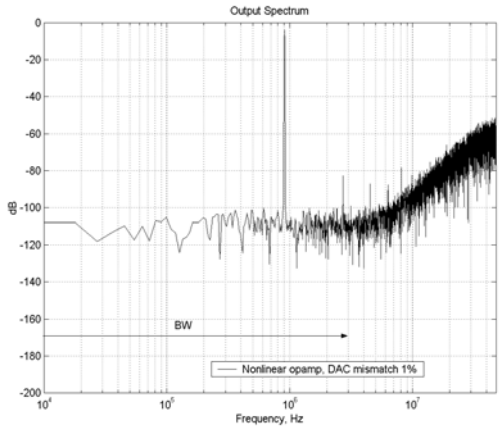
The feedback DAC is implemented as a thermometer coded unit-elements converter. Errors affecting the unit-elements of DAC are controlled by a variable that determines the standard deviation of the Gaussian distribution of the errors.



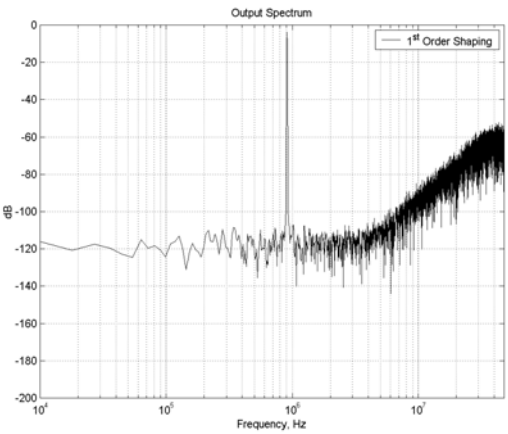
a. Traditional 3rd order 5-bit ΣΔ modulator



b. Proposed topology with ideal DAC



c. Proposed topology with 1% DAC error



d. Proposed topology with 1st shaping

Figure 3. Output spectrum for the 3rd order 5-bit ΣΔ modulators

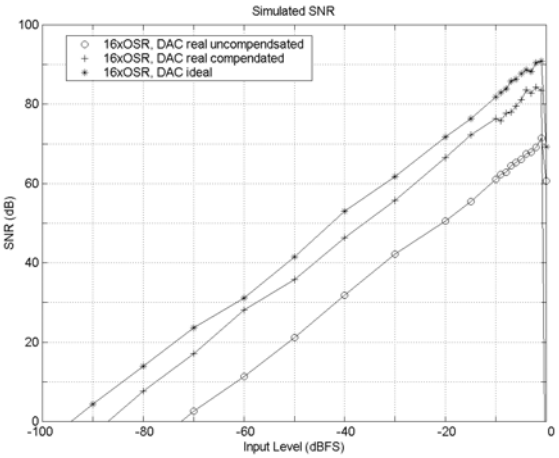


Figure 4. SNR vs. Input signal level

The input signal with a –6 dB 0.9 MHz sinusoidal wave was applied, the sampling frequency of the modulator was 96MHz, and the OSR was 16. The power spectral densities for the 3rd order Σ-Δ modulator topologies under the same condition are shown in Fig. 3. The traditional topology [10] implemented with nonlinear opamps and ideal DAC shows a low noise floor and the presence of input signal together with the 3rd harmonic (-65 dBFS) created due to the nonlinear opamps. The proposed topology implemented with nonlinear opamps and ideal DAC presents a low noise floor and an undistorted output, as in Fig. 3.b. Using a DAC with 1% mismatch error in the proposed topology, we can see an increased noise floor and harmonics of the input signal as in Fig. 3.c. The 3rd harmonic appears at –78 dBFS. Fig. 3.d shows an increased noise floor, but the presence of input signal without harmonics due to the 1st order mismatch noise shaping. These simulation results show that it can reduce the harmonic distortions from the nonlinear opamp by using the feedforward path.

Fig. 4 shows the simulated SNR of the proposed modulator against the input signal level. The plot shows the dynamic range being nearly 88 dB for a 3MHz bandwidth when for the feedback DAC the 1st order mismatch noise shaping has been used.

IV. CONCLUSION

In this paper, a new 3rd order multibit Σ-Δ modulator is presented. The feedforward signal path is used to reduce the opamp nonlinearity effects. In addition, performance degradation due to feedback DAC nonlinearity can be suppressed using a dynamic-element matching technique. By using the feedforward signal path and the multibit quantizer the 3rd order Σ-Δ modulator topology is a suitable candidate for wideband RF receivers. Simulation results show that an 84.7 dB peak SNDR can be achieved over a 3MHz signal bandwidth.

REFERENCES

[1] I. Fujimori et al., “A 2.5MHz Output-rate Σ-Δ ADC with 90 dB SNR and 102 SFDR”, in *Analog Circuit Design*, Boston: Kluwer Academic Publishers, 2000, pp. 95-117.

[2] P.G.A. Jespers, “Integrated converters: D to A and A to D Architecture, Analysis and Simulation”, Oxford University Press, 2001.

[3] I. H. H. Jorgensen, “A 3rd order low-power SI Sigma-Delta A/D converter for voice-band applications”, in *Proc. IEEE –ISCAS*, 1997, pp. 69-72.

[4] M. R. Miller and C. S. Perie, “A Multi-Bit Sigma-Delta ADC for Multi-Mode Receivers”, in *Proc. IEEE Custom Integrated Circuits Conference*, 2002, pp. 191-194.

[5] S. R. Norsworthy, R. Schreier and G.C. Temes, *Delta-Sigma Converters-Theory, Design and Simulation*, New York: IEEE Press, 1997, pp. 244-278.

[6] A. Rusu and H. Tenhunen, ”DAC nonlinearity effects in a wideband sigma-delta modulator architecture” in *Proc. IEEE-ASIC/SOC,* 2002, pp. 75-79.

[7] R. Schreier, “The delta-sigma toolbox 5.2 for Matlab”,1999, ftp://ftp.mathworks.com/ pub/contrib/v5/control/delsig

[8] J. Silva, U. J. Moon and G. C. Temes, “Wideband low-distortion delta-sigma ADC topology”, *IEE Electronics Letters*, no. 12, pp. 737-738, Jun. 2001.

[9] X. Wang, U. J. Moon, M. Liu and G. C. Temes, “Digital correlation technique for the estimation and correction of DAC errors in multibit MASH Delta-Sigma ADCs”, in *Proc. IEEE-ISCAS,* vol. 4, 2002, pp. 691-694.

[10] A. Yasuda, H. Tanimoto, and T. Iida, “A third-Order Σ-Δ Modulator Using Second-Order Noise-Shaping Dynamic Element Matching”, IEEE Journal of Solid-State Circuits, vol. 33, no. 12, 1998, pp. 1879-1886.