A Self-Calibration Technique for Monolithic High-Resolution D/A Converters

D. WOUTER J. GROENEVELD, HANS J. SCHOUWENAARS, SENIOR MEMBER, IEEE, HENK A. H. TERMEER, AND CORNELIS A. A. BASTIAANSEN

Abstract—**A self-calibration technique based upon charge storage on the gate–source capacitance of CMOS transistors is presented. The technique can produce multiple copies of a reference current. Therefore, it is suitable for the calibration of high-resolution D/A converters which are based upon equal current sources. As the storage capacitor is internal, no external components are required. A calibrated spare current source is used to allow continuous converter operation. This implies that no special calibration cycles are required. To show the capabilities of the calibration technique, it was implemented in a 16-bit D/A converter. Measurement results of the converter show a total harmonic distortion of 0.0025 percent at a power consumption of 20 mW and a minimum supply voltage of 3 V. The design was fabricated in a 1.6-μm double-metal CMOS process without special options.**

I. Introduction

NOWADAYS, the demands on the linearity of high-resolution D/A and A/D converters for measurement equipment and digital audio are so high that the achievable accuracy based upon matching of components in a standard process is not sufficient. Therefore, additional calibration techniques are used to achieve high resolution. A disadvantage of many calibration techniques is the need for a special calibration period [1]. During this period, the converter cannot be used for conversion, which particularly limits the application range. Furthermore, a relatively large chip area is needed to store the error signals. Other calibration techniques like laser trimming [2] and external adjustment take precious time and facilities and are sensitive to aging and temperature, while dynamic element matching [3], [4] needs external components. In this paper, a self-calibration technique is presented which needs no calibration period, additional trimming, or external components, and is insensitive to process variations. The technique is implemented in a standard CMOS process, which is also the best process choice for low power consumption.

Manuscript received May 3, 1989; revised August 22, 1989.
The authors are with Philips Research Laboratories, 5600 JA Eindhoven, The Netherlands.
IEEE Log Number 8931439.

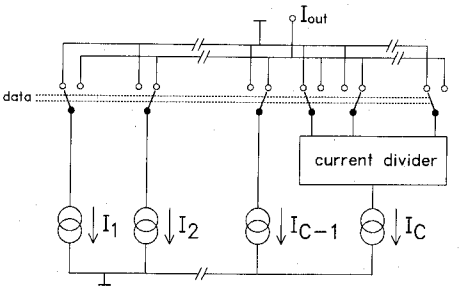


Fig. 1. Basic circuit diagram of current-dividing D/A converter.

II. Linearity Considerations

Fig. 1 shows the basic block diagram of an N-bit segmented D/A converter. An array of C coarse current sources is shown, which all deliver the same output current. To increase the resolution, one of the coarse currents, in this case I_c, can be divided into more fine current levels by a passive current divider. Depending on the value of the data signal, a number of the currents are switched to the output terminal I_{out}, and the remaining currents are dumped to signal ground. It was shown before that a resolution up to 10 bit can be obtained by a passive divider stage [5]. To obtain a higher resolution, the addition of the equal coarse current sources is necessary ($C = 64$ for 16 bits). In that case the linearity of the converter depends mainly on the mutual equality of the coarse currents, which may differ less than half a LSB current to achieve a maximum linearity. Since it is impossible to obtain a 16-bit accuracy with standard CMOS components [6], [7], the new calibration technique is essential to make this type of converter architecture feasible.

III. Basic Calibration Principle

First, the calibration principle for one single current source will be described, and later on this will be extended to a larger number of current sources.

The basic circuit of a current cell is shown in Fig. 2. When the switches S_1 and S_2 are in the depicted state, a

0018-9200/89/1200-1517$01.00 ©1989 IEEE

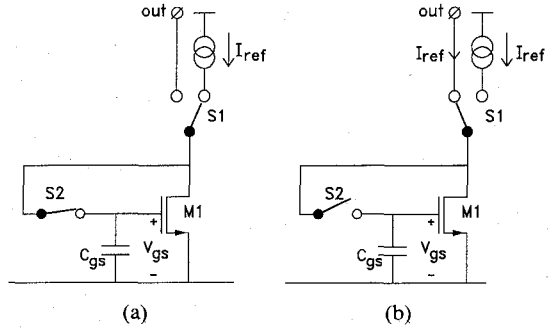


Fig. 2. Calibration principle. (a) Calibration. (b) Operation.

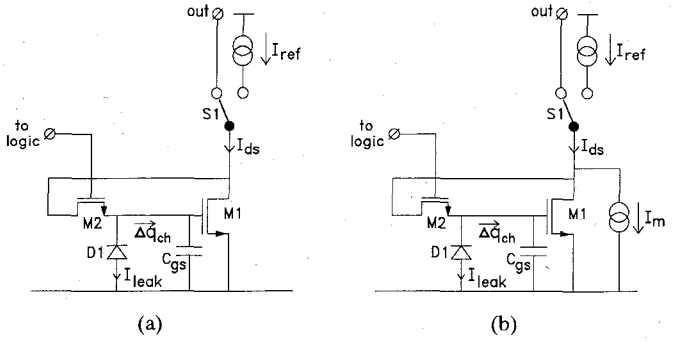


Fig. 3. (a) Real calibration circuit. (b) Improved calibration circuit.

reference current I_{ref} flows into transistor M_1, as it is connected as an MOS diode. The voltage V_{gs} on the intrinsic gate–source capacitance C_{gs} of M_1 is then determined by the transistor characteristics. When S_2 is opened and S_1 is switched to the other position, the gate-to-source voltage V_{gs} of M_1 is not changed since the charge on C_{gs} is preserved. Provided that the drain voltage is not changed either, the drain current of M_1 will still be equal to I_{ref}. This current is now available at the I_{out} terminal, and the original reference current source is no longer needed.

IV. Imperfections

In practice, the switches S_1 and S_2 are MOS transistors as shown in Fig. 3(a). This gives rise to some disturbing effects, which cause changes in the gate voltage of M_1 during switching.

When M_2 is switched off, its channel charge q_{ch} is partly dumped on the gate of M_1, and so the charge on C_{gs} of M_1 is decreased by an amount Δq_{ch}. The charge change implies a sudden decrease of V_{gs} of M_1:

$$\Delta V_{gs,q} = \frac{\Delta q_{ch}}{C_{gs}}. \tag{1}$$

After switching, another effect influences V_{gs}. Although M_2 is switched off, the reverse-biased diode D_1 between its source and the substrate is still present. The leakage current I_{leak} of this diode decreases the charge on C_{gs} continuously. Assuming that calibration is done at $t = 0$, the gate voltage equals

$$V_{gs,\text{leak}}(t) = V_{gs}(0) - \frac{I_{\text{leak}}}{C_{gs}} t. \tag{2}$$

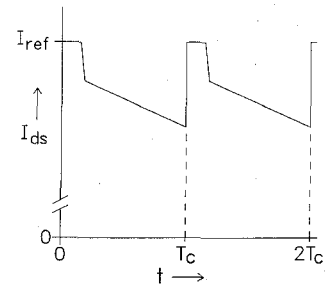


Fig. 4. Drain current I_{ds} of M_1 versus time.

The changes in the gate voltage of M_1 are transformed into changes in the drain current I_{ds} by its transconductance g_m. The output current is represented by the solid line in the graph of Fig. 4. The voltage drop described by (1) causes a drop in the output current just after calibration:

$$I_{ds,q} = I_{\text{ref}} - g_m \Delta V_{gs,q} = I_{\text{ref}} - g_m \frac{\Delta q_{ch}}{C_{gs}}. \tag{3}$$

The transconductance of M_1 equals

$$g_m = \sqrt{2\mu C_{ox} \frac{W}{L} I_{ds}} \tag{4}$$

where μ represents the electron mobility and C_{ox} the oxide capacitance per square micrometer.

The gate–source capacitance can be rewritten as

$$C_{gs} = \tfrac{2}{3} WLC_{ox}. \tag{5}$$

Substituting (4) and (5) into (3) yields

$$I_{ds,q} = I_{\text{ref}} - \frac{3}{2} \sqrt{\frac{2\mu}{C_{ox}}} \cdot \frac{\Delta q_{ch}}{L} \sqrt{\frac{I_{ds}}{WL}}. \tag{6}$$

The leakage effect in the drain current can be calculated in the same way. The time-dependent drain current due to the diode leakage (2) is

$$I_{ds,\text{leak}}(t) = g_m V_{gs,\text{leak}}(t) = I_{\text{ref}} - g_m \frac{I_{\text{leak}}}{C_{gs}} t. \tag{7}$$

Substitution of (4) and (5) into (7) yields

$$I_{ds,\text{leak}}(t) = I_{\text{ref}} - \frac{3}{2} \sqrt{\frac{2\mu}{C_{ox}}} \cdot \frac{1}{L} \sqrt{\frac{I_{ds}}{WL}} I_{\text{leak}} t. \tag{8}$$

This formula implies that after a certain time T_c the current cell has to be calibrated again to keep its output current within a specified range.

The results of (6) and (8) clearly indicate that the ratio μ/C_{ox} should be small to keep the changes in the drain current small, so an advanced CMOS process is preferable. In addition, both equations contain parameters that can be influenced by the actual design.

All adjustable parameters have limits that depend on other considerations as well. The current I_{ds} is determined by the properties of the circuit in which the current cell has

to be implemented. The transistor width and especially its length should be as large as possible for optimal calibration and $1/f$ noise behavior, but this is limited by layout size considerations that become more important when many cells are used. Furthermore, the W/L ratio has a minimum because of limits on V_{gs}. In the following calculations, a maximum V_{gs} of 1.5 V is taken, and the rms value of thermal plus $1/f$ noise over the audio band of one current is designed to be 100 dB below its dc value. Note that for N currents, the ratio between total dc value and noise will improve by a factor of $\sqrt{N}$, so the mentioned 100 dB is sufficient for very high-resolution D/A converter design.

To value the importance of the dumped channel charge q_{ch}, one must realize that the equality of the output current of two or more cells is of major importance, and not the ratio between output current and the reference current. This implies that only differences $\Delta I_{ds,q}$ in the current drop as described in (6) must be taken into account. So, differences in Δq_{ch} due to switch mismatches and differences in the transconductance of the current-source transistors do influence the mutual equality of output currents. The switch mismatches are determined by the switch sizes. However, these must be kept minimal to keep I_{leak} small. Therefore, a relatively large mismatch in channel charge has to be expected.

To evaluate the feasibility of the calibration technique, the following values are taken:

$$I_{ds} = 10\ \mu\text{A},$$
$$C_{ox} = 1.4\ \text{mF/m}^2,$$
$$W_1/L_1 = 25\ \mu\text{m}/30\ \mu\text{m},$$
$$W_2/L_2 = 2.4\ \mu\text{m}/1.6\ \mu\text{m},$$
$$I_{\text{leak}} = 10\ \text{mA/m}^2.$$

Furthermore, a difference in g_m of 2 percent and a difference in Δq_{ch} of 10 percent are taken into account. Now (6) yields

$$\Delta I_{ds,q} \approx 5\ \text{nA} \tag{9}$$

and (8) gives

$$I_{ds,\text{leak}}(t) \approx I_{\text{ref}} - 23 \cdot 10^{-6} t. \tag{10}$$

When a 10-bit current divider stage is used in the basic block diagram of Fig. 1, the LSB current is about $2^{-10} I_{ds} \approx 10$ nA. This means that all output currents have to be accurate within 5 nA. Equation (9) shows that this is almost realized. However, (10) implies that for this accuracy, the calibration repetition time T_c equals 217 μs. This results in a quite high calibration rate when many cells have to be calibrated.

V. Improved Calibration Technique

A very simple addition to the circuit of Fig. 3(a) is shown in Fig. 3(b). In parallel to the current-source transistor M_1, a main current source I_m is added which has a value of about 90 percent of the reference current. This decreases the value of M_1's current to about 10 percent, so its transconductance is decreased by a factor of $\sqrt{10}$. Furthermore, the size of M_1 can now be optimized to $W/L = 10\ \mu\text{m}/75\ \mu\text{m}$ since I_{ds} is smaller. In this way, it is possible to reduce g_m by a factor of 8 while keeping C_{gs} of M_1 at the same value.

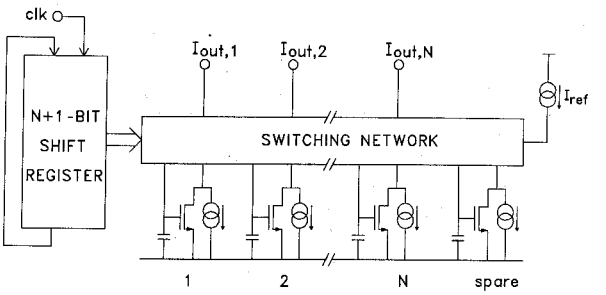


Fig. 5. Block diagram for the generation of N equal continuously flowing currents.

The main current source I_m is easy to implement: since its value may vary a few percent, it can be derived from the reference current by simple current mirrors. Unfortunately, this causes a larger mismatch of g_m between several cells since $I_{\text{ref}} - I_m$ can deviate about 30 percent. Therefore, in this case the absolute value of the injected charge q_{ch} must be minimized as well as Δq_{ch}, for instance by adding a compensation transistor to the switch transistor M_2. The calculated results of (6) and (8) now become

$$\Delta I_{ds,q} \approx 1.2\ \text{nA} \tag{11}$$

$$I_{ds,\text{leak}}(t) \approx I_{\text{ref}} - 3.0 \cdot 10^{-6} t. \tag{12}$$

Clearly, the accuracy is sufficient, while the repetition period T_c is increased to 1.67 ms.

VI. Continuous Current Calibration

To make the calibration technique suitable for the design of a D/A converter, it must be extended to an array of current sources. Therefore, the calibration period, in which a current cell does not operate normally, must be made invisible at the current outputs of the array. This is realized by the continuous current calibration principle which is shown in Fig. 5. The principle is characterized by the presence of $N+1$ current cells, that generate N equal output currents. The selection of the cell to be calibrated is done by an $N+1$-stage shift register, shown at the left side. Some logic takes care that only one stage contains a logic ONE, while the other outputs are ZERO. Round coupling ensures that after sequentially calibrating all cells, the first cell is calibrated again, and so on. The switches of all current cells are incorporated in the switching network. This network connects all the output currents of the normally functioning cells to their corresponding outputs. The one cell under calibration is connected to the reference current. Because this cell is now not delivering any current to its output terminal, the output current of the spare cell is switched to this terminal. In this way it is guaranteed

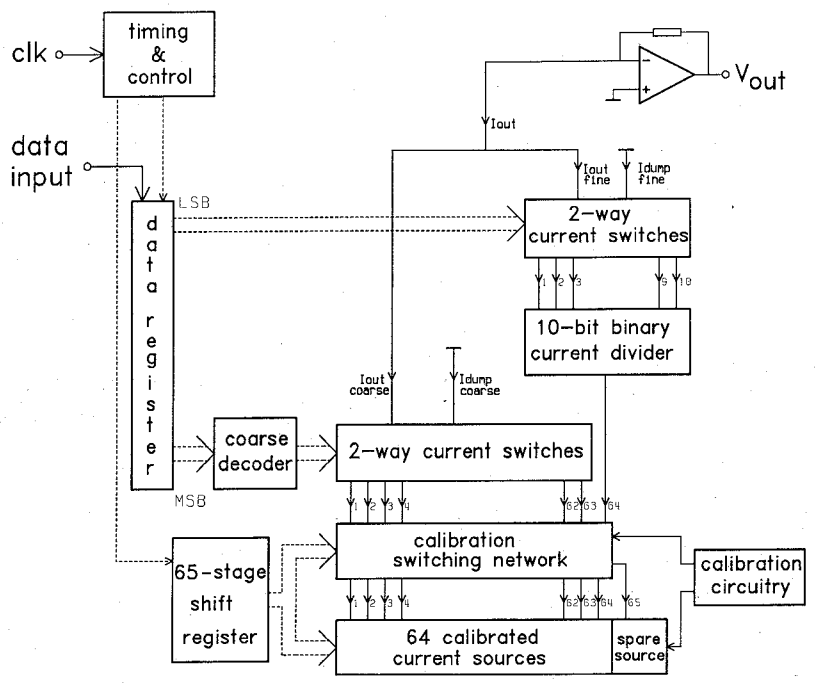


Fig. 6. Block diagram of the 16-bit calibrated D/A converter.

that there are always N equal currents available at the output terminals, so the need for special calibration cycles is eliminated.

VII. D/A Converter Architecture

To investigate the suitability of this technique for high-resolution D/A conversion, a 16-bit D/A converter was designed that meets the demands for digital audio. The basic block diagram is shown in Fig. 6. The design is based upon 64 equal current sources. Each current source is in fact a complete current cell having the basic architecture of Fig. 3(b). A 65-bit shift register selects the cells one by one for calibration. The calibration circuitry consists mainly of the reference source and will be described in detail later on. The current outputs of 63 normally functioning cells are fed to 63 two-way current switches, and one cell is directly connected to a 10-bit binary current divider. Depending on the input data, a number of the 64 currents are switched to the output line, and the rest of the 64 currents are dumped to signal ground. In this way, 64 accurate output current levels can be realized. The intermediate levels are obtained by adding a well-defined part of the 64th current generated by the calibration network. This part is realized by dividing this current into binary-weighted levels by means of a 10-bit current divider [5]. The divider output currents are then switched to the output line or to signal ground by two-way current switches, which are directly controlled by the ten least significant data bits. Finally, the output current is converted into a voltage by means of an external operational amplifier and a resistor. To reduce the supply voltage, all current switches are designed for a small voltage drop (< 50 mV). Due to the parallel structure the minimum supply voltage is only 3 V.

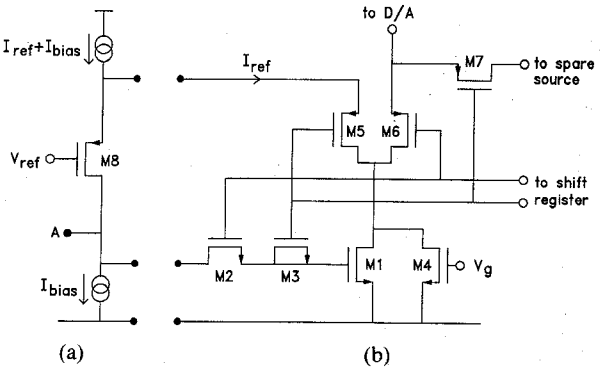


Fig. 7. (a) Calibration circuitry. (b) Current cell.

VIII. Calibration Circuitry

Fig. 7(a) shows the common part of the calibration circuitry. It consists of the reference current source which is applied externally, one PMOS transistor M_8, and two bias current sources. Fig. 7(b) shows one of the 64 cells and a part of the switching network. The dotted nodes are connected to all cells and to the calibration circuitry. Each cell has a main current source, consisting of one NMOS transistor M_4. The gate voltage V_g of M_4 is common for all cells.

In normal operation, the PMOS switch M_6 connects the current sources M_1 and M_4 to the output terminal. When the cell is calibrated, the shift register selects the cell by raising its "select" signal, and disconnects the cell from the D/A by routing the current through M_5 instead of M_6. M_5 is also a PMOS switch operating in the linear region. The spare source is now routed to the D/A through M_7. The loop between drain and gate of M_1 is closed by three transistors. The first is M_5, followed by the level shifter M_8, which is biased by a noncritical current I_{bias}. Finally,

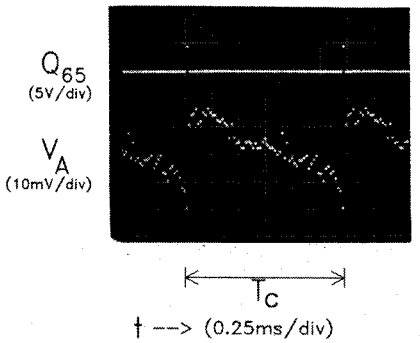


Fig. 8. Oscilloscope photograph.

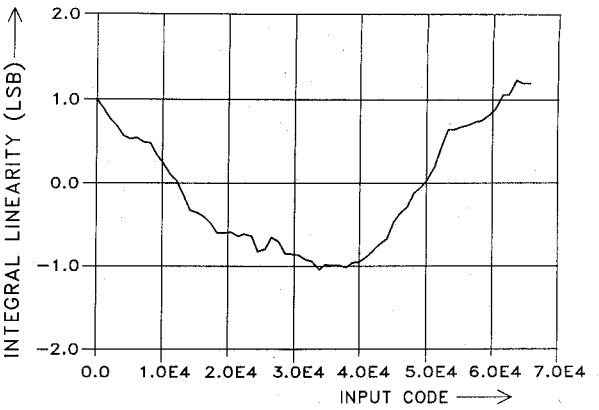


Fig. 9. Measured integral linearity of the 16-bit DAC.

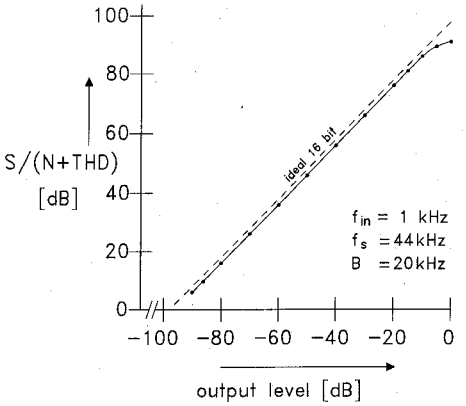


Fig. 10. Distortion performance of the 16-bit DAC.

the compensated switch M_2/M_3 closes the loop. M_3 is added to reduce the absolute amount of charge injection of the M_2/M_3 switch.

The level-shift stage consisting of M_8 and the bias current sources ensures that the drain voltages of M_1 and M_4 are the same during operation and calibration. During operation, this voltage is determined by the D/A circuit. During calibration, the drain voltage of the current sources is equal to the source voltage of M_8 within some millivolts since the voltage drop across switch M_5 is that small. The source voltage of M_8 is determined by V_{ref} and I_{bias} and is thus stable. In this way, the drain voltages of M_1 and M_4 can be kept at the same potential during calibration and operation, since they no longer depend on the gate voltage of M_1, as is the case in Fig. 2.

The clock frequency of the shift register is chosen to be equal to the audio sampling frequency, i.e., 44.1 kHz. The resulting calibration period T_c for each of the 65 current cells equals 1.5 ms.

IX. Measurement Results

The operation of the whole calibration circuit can be clarified by the oscilloscope photograph of Fig. 8. The top trace shows the output signal of the last shift-register stage, which marks the calibration period of the spare source. The lower trace shows the different gate voltages of the M_1 transistors on node A in Fig. 7(a). The dc amplitude of this signal is about 1.5 V, and the sawtooth-like ripple has an amplitude of 40 mV. It is clear that in this case a linear gradient is present on the main current-source array, since the voltages on node A give an impression of the difference between the reference current value and the main current-source values. Calculations show that in this case the original mismatch over the current-source array equals 0.5 percent. So, without calibration the converter would yield a harmonic distortion performance of 0.13 percent.

The measured integral linearity of the 16-bit D/A converter is shown in Fig. 9. As can be seen, the integral linearity is within two 16-bit LSB's. In the flat part in the middle of the curve the linearity is much better. This indicates that the converter is very well suited to digital audio, since in this application field a good linearity for small signals is absolutely needed. This is also visible in Fig. 10, which shows the measured ratio between the rms value of the wanted signal versus the rms value of the error signal which includes noise, harmonics, and spurious components. The measurement was performed using an HP 339A distortion measurement set. Measuring bandwidth is 20 Hz to 20 kHz. No dependence on temperature (-10 to 70°C) or on frequency of the input sine wave was found. Frequency components related to the refreshment of the individual current cells are all below -110 dB, thus not affecting the dynamic range of the converter. At lower signal levels up to -10 dB, the converter has a real 16-bit performance. At higher signal levels, some deviation from the theoretical curve is measured due to the nonideal absolute linearity.

A microphotograph of the test circuit is shown in Fig. 11. Easily, a distinction can be made between the 6-bit coarse part and the 10-bit fine part. The modular design approach has resulted in a very regular layout. Most of the bonding pads are added for test purposes. Finally, the most important specifications of the converter are listed in Table I.

X. Conclusion

A self-calibration technique is used to realize an array of current sources which are equal to each other within 0.02 percent. The calibration of an MOS current source is done by biasing it with a reference current. After that, the gate

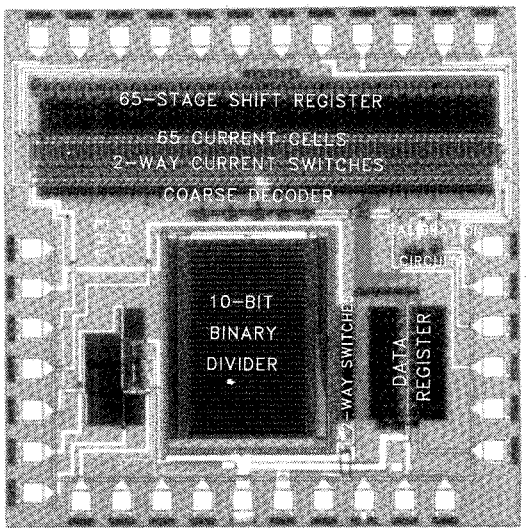


Fig. 11. Die photograph of the 16-bit DAC.

TABLE I
D/A CONVERTER SPECIFICATIONS

resolution	16 bit
dynamic range	94 dB
S/(N+THD) at 0dB	92 dB
at -10dB	84 dB
supply voltage range	3 to 5 V
power dissipation	20 mW at 5 V
temperature range	-10 to 70° C
process	1.6 μm CMOS
active chip area	2.8 mm^2

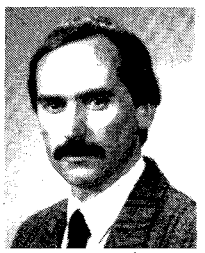
is disconnected from the biasing circuit and since the gate-to-source voltage is not changed, the value of the output current of the current source equals the reference value. To reduce the sensitivity for clock feedthrough in switches and for diode leakage currents, calibration is done only on the difference between a main current source and the reference current. The array of calibrated sources is extended with a spare source to ensure that enough calibrated currents are available at any time. The technique can be used in any application that requires equal currents. As an example, a 16-bit CMOS D/A converter for digital audio was designed in which the technique was incorporated. Measurement results show a linearity of 0.0025 percent at a power dissipation of 20 mW, a minimum supply voltage of 3 V, and an active chip area of 2.8 mm^2.

REFERENCES

[1] H. S. Lee, D. A. Hodges, and P. R. Gray, "A self-calibrating 15b CMOS A/D converter," *IEEE J. Solid-State Circuits*, vol. SC-19, pp. 813–819, Dec. 1984.
[2] J. R. Naylor, "A complete high-speed voltage output 16-bit monolithic DAC," *IEEE J. Solid-State Circuits*, vol. SC-18, pp. 729–735, Dec. 1983.
[3] R. J. van de Plassche, "Dynamic element matching for high-accuracy monolithic D/A converters," *IEEE J. Solid-State Circuits*, vol. SC-11, pp. 795–800, Dec. 1976.
[4] H. J. Schouwenaars, E. C. Dijkmans, B. M. J. Kup, and E. J. M. van Tuijl, "A monolithic dual 16-bit D/A converter," *IEEE J. Solid-State Circuits*, vol. SC-21, pp. 424–429, June 1986.
[5] H. J. Schouwenaars, D. W. J. Groeneveld, and H. A. H. Termeer, "A low-power stereo 16-bit CMOS D/A converter for digital audio," *IEEE J. Solid-State Circuits*, vol. 23, pp. 1290–1297, Dec. 1988.
[6] M. J. M. Pelgrom and A. C. J. Duinmaijer, "Matching properties of MOS transistors," in *ESSCIRC Dig. Tech. Papers*, Sept. 1988, pp. 327–330.
[7] Y. Yamada, M. Kajitani, and T. Ohgishi, "A 16-bit CMOS D/A converter for digital audio applications," *IEEE Trans. Consumer Electron.*, vol. CE-33, pp. 267–273, Aug. 1987.

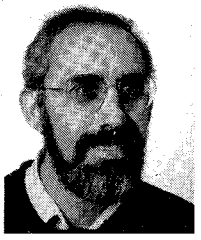
D. Wouter J. Groeneveld was born in Rotterdam, The Netherlands, on February 28, 1962. In 1986 he received the Ir. degree in electrical engineering from the Delft University of Technology, Delft, The Netherlands.

In that same year he joined Philips Research Laboratories, Eindhoven, The Netherlands, where he is working in the field of high-resolution D/A and A/D converters and associated circuits for digital audio.



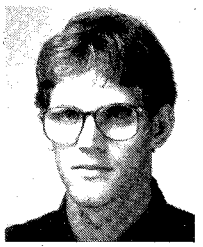
Hans J. Schouwenaars (SM'89) was born in Rotterdam, The Netherlands, on October 9, 1954. He received the B.S. degree in electrical engineering from the Hogere Technische School, Dordrecht, The Netherlands, in December 1978 and the degree of master of philosophy from the University of Wales, United Kingdom, in 1989.

In 1978 he joined the Analog Integrated Electronics Group of the Philips Research Laboratories, Eindhoven, The Netherlands, where he is working on the design of integrated circuits in bipolar and CMOS processes such as operational amplifiers, reference sources, high-performance sample-and-hold amplifiers, and high-resolution analog-to-digital and digital-to-analog converters for digital audio applications.



Henk A. H. Termeer was born in Sint Oedenrode, The Netherlands, on February 29, 1948. He received the degree in electrical engineering from the Eindhoven Technical College, Eindhoven, The Netherlands, in 1967.

In 1970 he joined Philips Research Laboratories, Eindhoven, The Netherlands, where he is engaged in electrical engineering and IC design of MOS and bipolar circuits in the Analog Integrated Electronics Group.



Cornelis A. A. Bastiaansen was born in Breda, The Netherlands, on August 4, 1962. He received the B.S. degree in electrical engineering from the Technical College, Breda, The Netherlands, in 1985.

In that same year he joined the Philips Research Laboratories, Eindhoven, The Netherlands. After working for two years in the field of photolithography, he is presently engaged in the design of AD/DA converters for video and digital audio applications.