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Telex: 066-6491 • FAX (520) 889-1510 • Product Info: (800) 548-6132 • Internet: www.burr-brown.com/ • FAXLine: (800) 548-6133

SUPERPOSITION: THE HIDDEN DAC LINEARITY ERROR

As More DACs Become Available With Resolutions of 12 Bits and Greater, Users Should Know the Causes and Effects of Superposition Error on Relative and Absolute Accuracy and What to Do to Minimize It.

A digital-to-analog converter (DAC) translates digital signals to analog signals. For example, a 12-bit DAC takes a 12-bit binary number, called an input code, and converts it into one of 4,096 analog output voltages or currents. When the contribution to the output voltage or current of each individual bit is independent of any other, it means that the device exhibits no superposition error or that "superposition holds." For a DAC with little or no superposition error, the linearity error for any given code will relate to the linearity error at some different code. This allows you to determine the worst case linearity error, and the digital code where that error occurs, with a very simple test.[1]

However, if the DAC under test has excessive superposition error, this simple test will give erroneous results; therefore, you must test all digital codes to determine the worst case error and code. Superposition error, or bit interaction, often is significant in converters with a resolution of 12 to 16 bits. If the error becomes large enough, a DAC may fail to meet a 1/2LSB linearity error or relative accuracy specification even with each individual bit adjusted perfectly. This specification becomes important in many applications such as automatic test equipment or precision voltage standards where the absolute value of the output voltage must remain within specified limits after calibration of offset and gain errors.

For a DAC with low superposition, the following equation determines the output voltage, if we assume that the offset and gain errors have been removed:

$$V_O = V_{FS}\left[\begin{matrix} b_1(1/2+\varepsilon_1)+b_2(1/4+\varepsilon_2)+\ldots \\ +b_n(1/2n+\varepsilon_n)\end{matrix}\right], \quad (1)$$

where $\varepsilon\iota \times V_{FS}$ equals the linearity error associated with the i^{th} bit and b_i, equals the value (0 or 1) of the i^{th} bit of the DAC input code. Since the analog output error with all input code bits off (000...000) and all input bits on (111...111) has been adjusted to 0 the summation of all the bit errors,

$$(\varepsilon_1+\varepsilon_2+\varepsilon_3\ldots\varepsilon_n)\text{ or }\left(\sum_{i=i}^{n}\varepsilon_i\right), \quad (2)$$

becomes zero. This means that the errors are symmetrical or, in other words, for every possible input code there exists an equal and opposite error associated with the one's complement of that code. The linearity error (sometimes called relative accuracy, integral linearity, nonlinearity or endpoint linearity) is defined as the maximum error magnitude that occurs.

Now consider the relationship between the individual bit errors (ε_i) and the linearity error. There exists some digital input code (b_1, b_2 . . . b_n) that yields the maximum linearity error (E_{MAX}) and the one's complement of this code (b_1, b_2...b_n), that must yield an error of the same magnitude but in the opposite direction ($-E_{MAX}$). The relative magnitude and polarities of the errors determine which actual input code has the most linearity error. For the error to be maximum, all of the error terms must be additive and the following proves true:

$$\begin{aligned} |E_{MAX}|+|-E_{MAX}| &= |b_1\varepsilon_1+b_2\varepsilon_2+\ldots \\ &\quad +b_n\varepsilon_n|+|\bar{b}_1\varepsilon_1+\bar{b}_2\varepsilon_2+\ldots+\bar{b}_n\varepsilon_n| \\ 2|E_{MAX}| &= (b_1+\bar{b}_1)|\varepsilon_1|+(b_2+\bar{b}_2)|\varepsilon_2|+\ldots \\ &\quad +(b_n+\bar{b}_n)|\varepsilon_n|; \end{aligned} \quad (3)$$

but $b_i + b_i = 1$, making the maximum linearity error:

$$|E_{MAX}| = 1/2\left[|\varepsilon_1|+|\varepsilon_2|+\ldots+|\varepsilon_n|\right]. \quad (4)$$

This result proves interesting because it relates the maximum linearity error to the individual bit errors; therefore, you can evaluate a DAC by simply measuring the output error associated with n digital input codes instead of all of the 2^n possible combinations.[2,3]

Stated another way, the sum of the positive bit errors should equal in magnitude the sum of the negative bit errors when the gain and offset errors have been removed. Any difference in these magnitudes indicates the presence of a superposition error. If this difference proves greater than approximately 1/10 of an LSB (JDEC standard for superposition error), further testing may become necessary to determine the accuracy of the DAC. However, a superposition error of more than l/10LSB does not by itself imply that a DAC cannot meet a linearity specification of, say, ±l/2LSB; it simply means that you must conduct a more elaborate test to determine the worst case linearity error and digital input code where that error occurs.

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A 3-BIT DAC

An example illustrating the relationship between linearity error and the individual bit errors for a 3-bit DAC appears in Figure 1a. Any deviation in the DAC output from the straight line drawn between all bits off and all bits on indicates a linearity error. With the superposition error less than 1/10LSB, the error pattern will appear as symmetrical around midscale as indicated.

Figure 1b shows a transfer characteristic for a 3-bit DAC which exhibits superposition error. Note that, in this example, the symmetrical error pattern around midscale no longer exists. You must consider the difference between the electrical sum and the algebraic sum of the bit errors when determining whether to use a more comprehensive test.

The data in Table I came from a 12-bit hybrid DAC. Note that, for this test, the full scale voltage was increased to 10.2375V, making the ideal bit weights, starting at the LSB, equal to 2.5mV, 5.0mV, l0.0mV... 2.560V, and finally 5.12V for the MSB. You can memorize these numbers easily and calculate the error voltages quickly by inspection. The difference between the algebraic sum of the positive bit errors (320µV) and negative bit errors (–310µV) equals only 10µV, which indicates a low superposition error. Thus, the maximum linearity error becomes 1/2 x (320 + 310) = 315µV.

The data in Table II came from a monolithic bipolar 12-bit DAC. Note that the difference here between the positive bit errors (+550µV) and the negative bit error (–1,650µV) equals –1.lmV or almost 1/2LSB. In this situation, superposition does not hold and you cannot say anything definite about linearity with the data available.

TESTING ALL INPUT CODES

When the short-cut method of measuring linearity error does not prove sufficient, you can develop a high speed measurement circuit capable of testing all 2^n code combinations. A simple schematic of this type of tester appears in Figure 2. The binary counter has n + 1 stages to provide a binary count from 0 to $2^n – 1$ and to reset the counters at the end of the count. The reference DAC and the x 10 error amplifier must have combined settling times to ±1/10LSB of less than 10µs since the system clock must operate at 20kHz to have a flicker-free display. For a 12-bit converter, a complete cycle takes 50µs x 4,096 counts or approximately l00ms. The output of the n^{th} counter stage also displays on the scope to indicate the midscale transition point, and offset and gain adjustment potentiometers are provided to zero the end points of the error display.

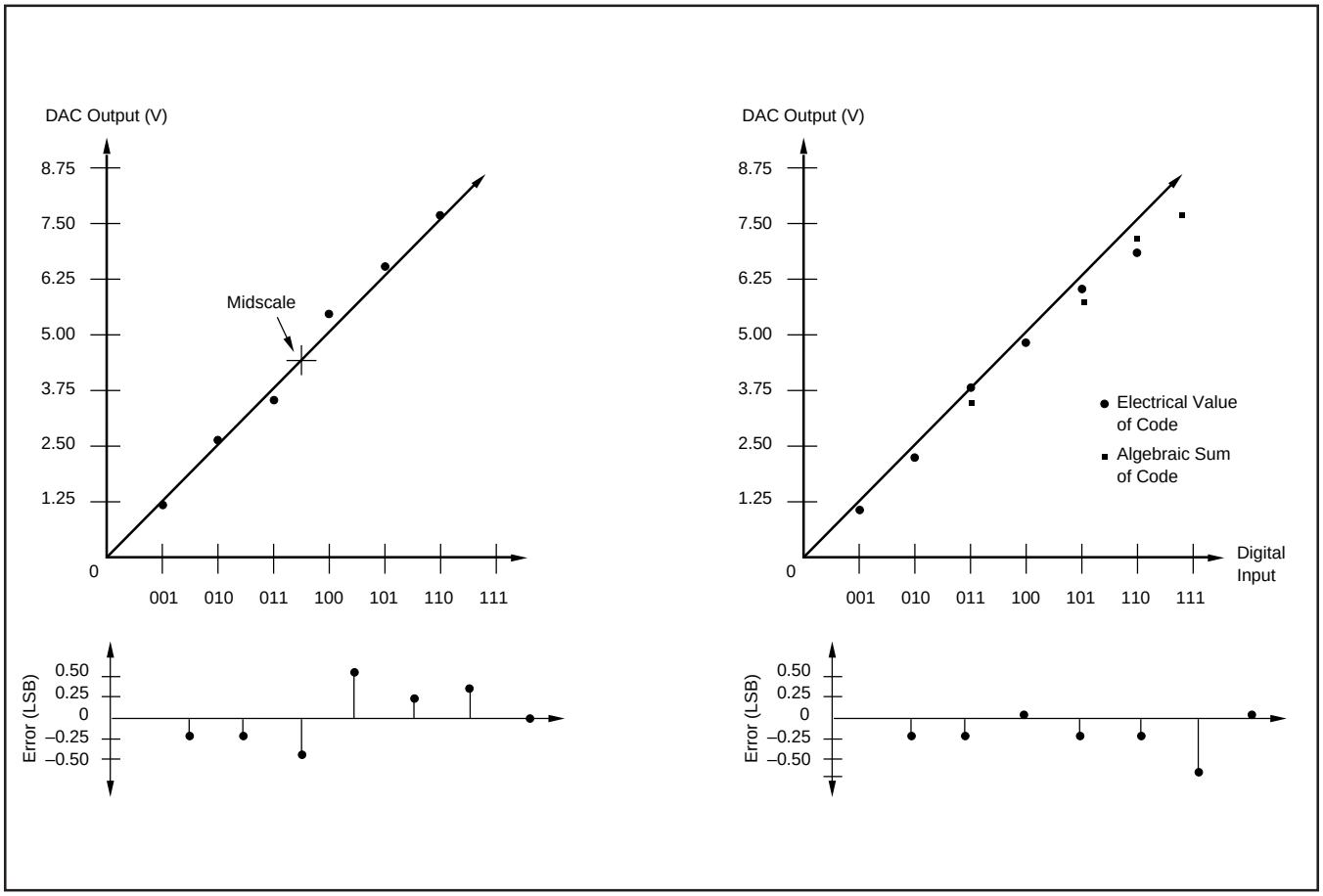

FIGURE 1. Both of These 3-Bit DAC Transfer Functions Exhibity Errors. Linearity Error (a) exists for input codes 001, 010, 101 and 110; note the symmetry of the errors about midscale. Superposition errors (b) lack symmetry about midscale.

INPUT CODE	IDEAL OUTPUT (V)	ACTUAL OUTPUT(V)	ERROR(μV)
All Bits "On"	+10.23750	+10.23750	0
All Bits "Off"	0	0	0
Bit 1 (MSB)	5.12000	5.11995	–50
Bit 2	2.56000	2.55982	–180
Bit 3	1.28000	1.27994	–60
Bit 4	0.64000	0.63998	–20
Bit 5	0.32000	0.32004	+40
Bit 6	0.16000	0.16004	+40
Bit 7	0.08000	0.08004	+40
Bit 8	0.04000	0.04005	+50
Bit 9	0.02000	0.02010	+100
Bit 10	0.01000	0.01002	+20
Bit 11	0.00500	0.00502	+20
Bit 12 (LSB)	0.00250	0.00251	+10
Positive Sum			+320
Negative Sum			–310
Difference			+10

TABLE I. In This Data from a 12-Bit Hybrid DAC, the Full-Scale Voltage Was Increased to 10.2375V, Making the Ideal Bit Weights, Starting at the LSB, Equal to 2.5mV, 5.0mV, 10.0mV...2.560V and Finally 5.12V for the MSB. You can easily memorize these numbers and quickly calculate the error voltages by inspection.

INPUT CODE	IDEAL OUTPUT (V)	ACTUAL OUTPUT(V)	ERROR(μV)
All Bits "On"	+10.23750	+10.23750	0
All Bits "Off"	0	0	0
Bit 1 (MSB)	5.12000	5.11927	–730
Bit 2	2.56000	2.55928	–720
Bit 3	1.28000	1.27996	–40
Bit 4	0.64000	0.64013	+130
Bit 5	0.32000	0.32013	+130
Bit 6	0.16000	0.16003	+30
Bit 7	0.08000	0.07987	–130
Bit 8	0.04000	0.03997	–30
Bit 9	0.02000	0.02000	0
Bit 10	0.01000	0.01008	+80
Bit 11	0.00500	0.00512	+120
Bit 12 (LSB)	0.00250	0.00256	+60
Positive Sum			+550
Negative Sum			–1650
Difference			–1100

TABLE II. Note That the Difference Between the Positivie Bit Errors (+550μV) and the negative bit errors (–1,650μV) in This Data from a Monolithic Bipolar DAC, Equals –1.1mV or Almost 1/2LSB. In this situation, superposition does not hold and you cannot say anything definite about linearity with the amount of data available.

This tester works well for 8-, 9-, and 10-bit converters. For a 12-bit DAC, the 4,096 segments displayed on the CRT are spaced so close together that the switching transients create a wide band of noise making it difficult to tell if the converter meets its specification, especially with a linearity error near the ±l/2LSB limit. One way around this problem, if you assume that the errors contributed by the last four bits of the DAC are small, entails inhibiting these bits with the AND gates shown in Figure 2; this reduces the binary count to 256 and also gives each count 16 times longer for the glitches to settle out. You can make other improvements to this tester such as automatic offset and gain error nulling, a sample/hold deglitcher to remove the glitches at the error output and a go/no go window comparator to test the linearity error at each binary count.

Using the test circuit shown in Figure 2, and three different 12-bit DACs produced the oscilloscopic photographs in Figure 3. The offset and gain errors have been nulled at the left and right portions of the photographs, respectively; and the linearity error appears as the deviation from the horizontal center line of the scope, with the vertical sensitivity l/2LSB per division. The digital input to the MSB indicates the mid-range and full-scale binary counts

The DAC errors displayed in Figure 3a appear symmetrically about the center of the scope, indicating very little superposition error; while those in Figure 3b are almost all positive which indicates a moderate amount of superposition error. Figure 3b shows why some manufacturers specify linearity error as the maximum deviation from a best fit straight line rather than straight line through the end points You can see, in this example, that a linearity error specification of ±l/2LSB proves easier to meet when using the best fit straight-line method. In a DAC with symmetrical error patterns, as shown in Figure 3a, a straight line through the end points becomes the same as a best fit straight line.

SOURCES OF SUPERPOSITION ERROR

Generally, superposition error in monolithic and hybrid converters results from the feedback resistor, R_f, changing in value as the output voltage varies from 0V to +10V. This apparent nonlinearity comes from the variable power dissipation that occurs in this resistor which can produce a temperature rise (self-heating) of as much as 1°C to 2°C in some DACs. This in turn changes the absolute value of the feedback resistor since it will have a temperature coefficient (TC) of between 50ppm/°C and 300ppm/°C for a thin-film material and over 1,000 ppm/°C for a monolithic diffused resistor. This problem generally does not occur in discrete data converters because the physical size of the feedback resistor is so large that the temperature rise, and therefore the resistance variation, remain extremely small. In a monolithic converter, however, with real estate at a premium, the mass of the feedback resistor is often so small the large temperature rise will occur for even small changes in power dissipation due to self-heating

To determine if the feedback resistor is at fault, substitute a low TC external resistor for the internal feedback resistor of the DAC and see if the nonlinearity disappears. The oscilloscope photograph in Figure 4 shows the results of using the test circuit shown in Figure 2, the same DACs whose transfer functions appear in Figures 3a and 3b respectively, with the internal feedback resistors being replaced by low TC external resistors. Note that the DAC errors in both cases are now almost evenly distributed about the center of the oscilloscope which indicates that the major cause of the superposition error has been removed. You cannot use an external feedback resistor, of course, in most practical applications because it will cause excessive gain drift since it will not track the internal diffused or thin-film reference resistor with variations in time and temperature.

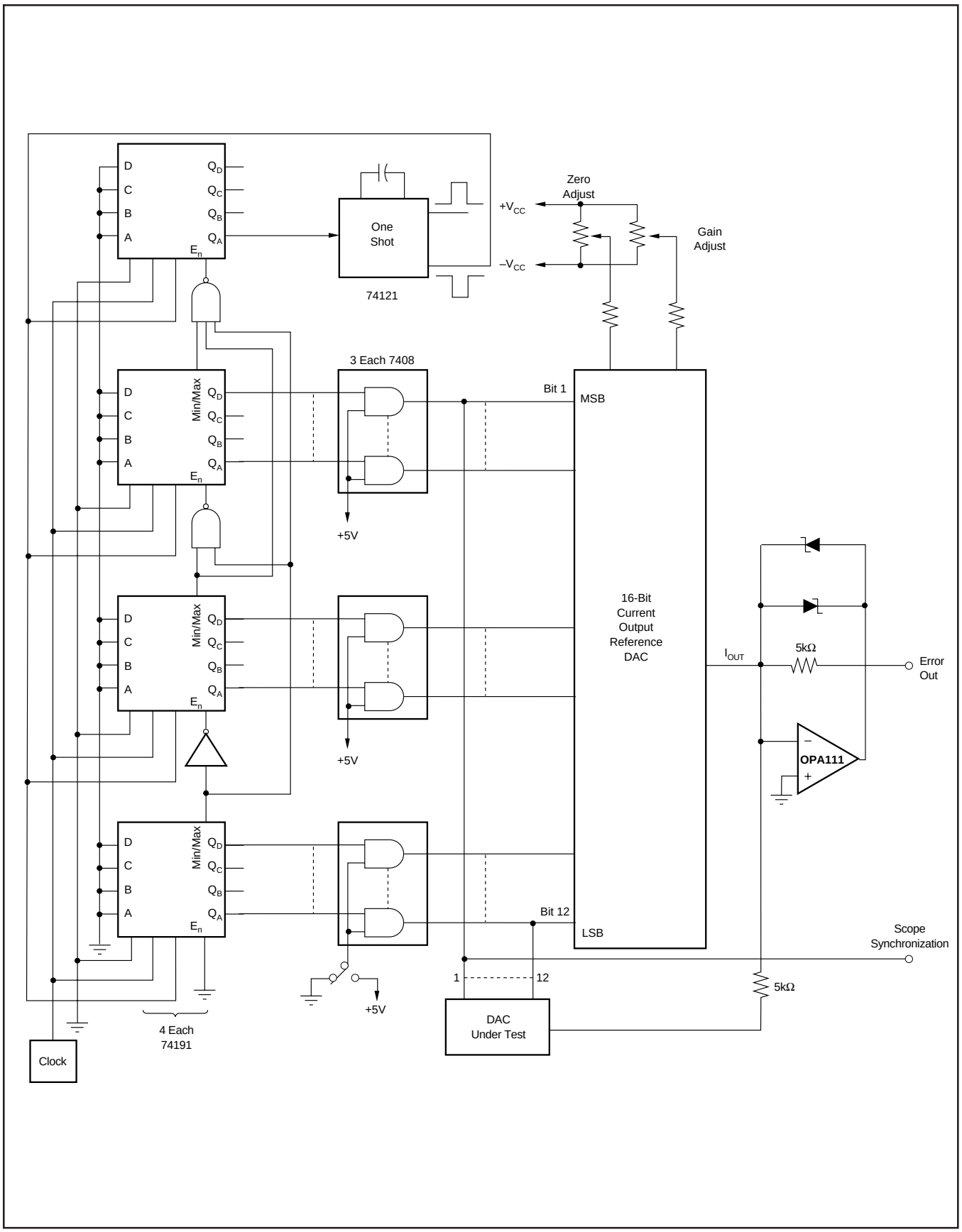

FIGURE 2. This Tester Works Well For 8-, 9-, and 10-Bit Converts. For a 12-bit DAC, the 4096, segments displayed on the CRT are spaced so close together that the switching transients create a wide band of noise making it difficult to tell if the converter meets its specification, especially with linearity error near the ±1/2LSB limit. One way around this problem, if you assume that the errors contributed by the last four bits of the DAC are small, entails inhibiting these bits with the AND gates shown.

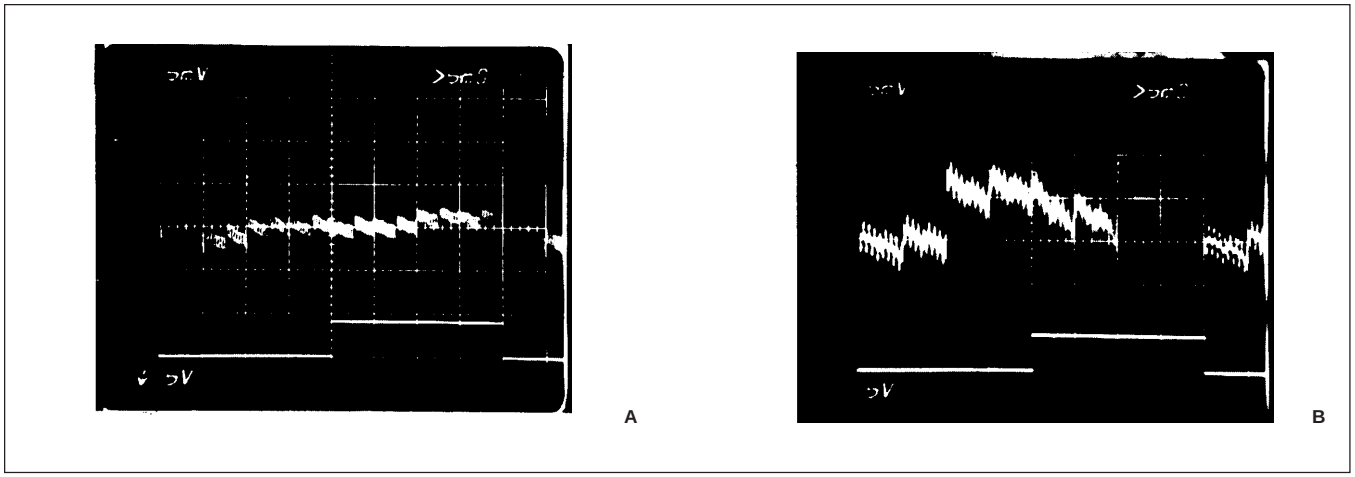

FIGURE 3. In These Scope Waveform Photographs Showing the Output of the Test Circuit in Figure 2, the Top Traces Indicate the Linearity Error, and the Bottom Traces Reflect the Status of the MSB of the Input Code. The Hybrid DAC (a) exhibits little superposition error, while the asymmetry of the linearity error (b) about midscale shows supersposition eror the monolithic bipolar DAC. The MSB transition marks the horizontal center.

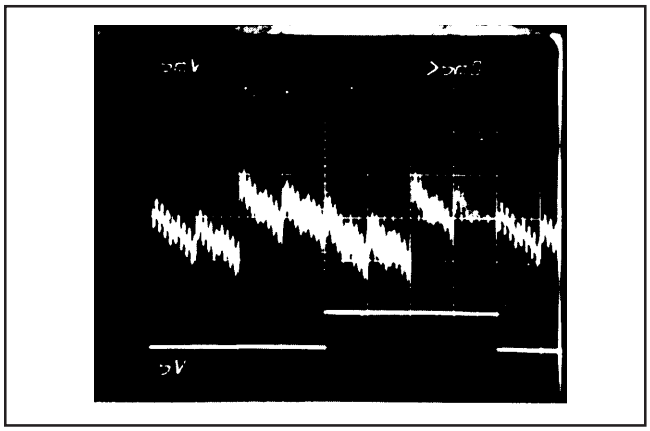

FIGURE 4. An External Feedback Resistor Can Decrease Superposition Error for the Monolithic Bipolar DAC Shown in Figure 3b.

Superposition error or bit interaction can occur in other ways—by temperature gradients on a monolithic chip which cause the magnitude of a bit output to be a function of the state of the other bit switches, or by feedback resistors which have an appreciable voltage coefficient of resistance (VCR), such as diffused resistors might. Again, the presence of superposition error does not mean a DAC will not meet its linearity specification, but you will need more extensive testing to verify if it does.

Superposition error, however, is by no means the only source of linearity error. Pay attention to your wiring whenever you use or test a DAC. When critical portions of a circuit share the same metallization path (e.g., a metallization path on a monolithic chip or in a wirebond; the contact resistance of a socket; or the wiring resistance of a test circuit), varying voltage drops caused by changing current levels can cause serious errors which could “drown out” any existing superposition error.

You can minimize the effect of wiring resistance (R_W,) external to the DAC by paying careful attention to the grounding and connection scheme employed. Figure 5a shows a correct connection configuration that you can use with most commercially available DACs to yield maximum accuracy. You can reduce or eliminate the effects of various wiring and contact resistances, R_1, R_2, R_3 and R_4, as follows:

• R_1 appears in series with the feedback resistance and therefore introduces only a gain error that can be nulled during calibration.

• R_2 appears inside the output amplifier feedback loop and the loop gain will reduce its effect.

• R_3 appears in series with the load resistor and will cause an error in the voltage across R_L. One-half LSB error would result at full load for $R_3 = 0.02\Omega$ for a 16-bit DAC. Therefore, if possible, you should sense the output voltage in such a way as to include R_3. Figure 5b illustrates the optimum connection made possible by the ground sense pin available on some higher accuracy DACs. In the configuration shown, $R'_F = R_F$ and $R_B = R_{DAC}$. This causes rejection of any signal developed across R_3 as a common mode input, and R_3 will not affect the voltage across R_L. This configuration will also reject noise present on the system common.

• R_4 remains negligible in both circuits with ground connections made as shown.

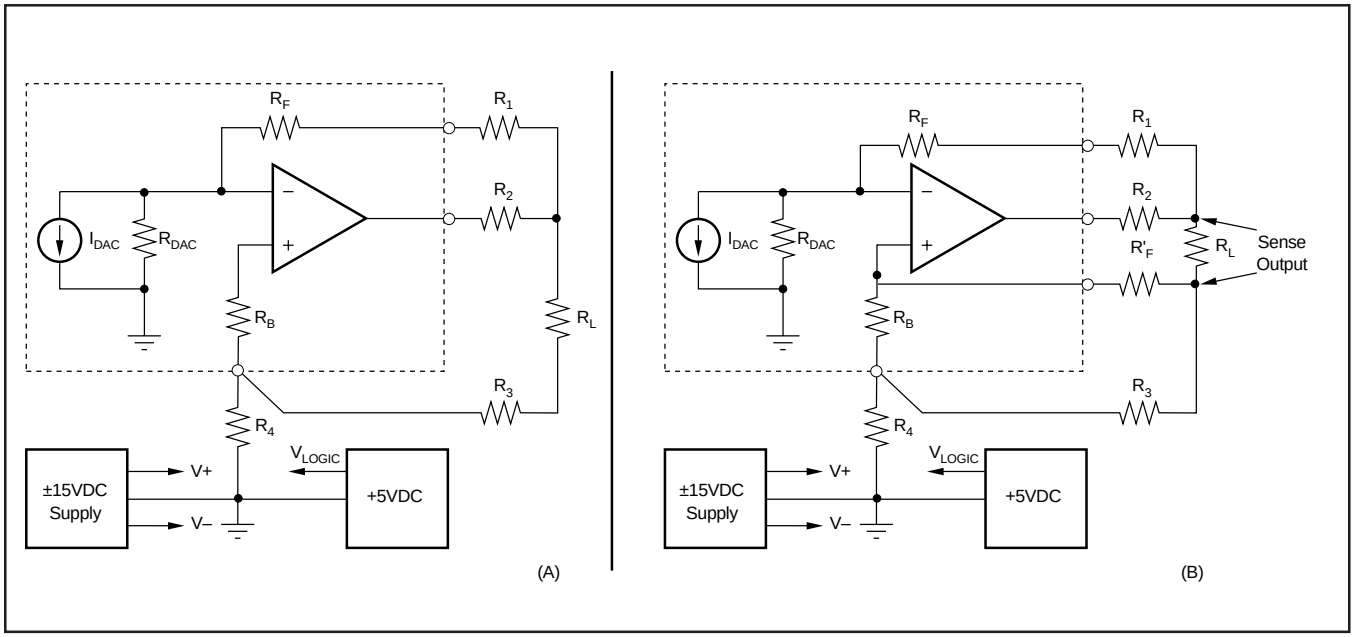

FIGURE 5. These Connection Diagrams Show How to Reduce the Effects of Wiring and Socket Resistance for a Typical DAC (a) and a High Accuracy DAC (b). Resistors R_1, R_2, R_3 and R_4 represent wiring and contact resistance.

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3. P. Prazak, "Progammable Handheld Calculator Computes Digital-to-Analog Converter Errors," pp.122-127, *Computer Design*, June 1978.

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