Measurement of Timing Jitter Contributions in a Dynamic Test Setup for A/D Converters

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***Abstract*—This article provides a new method which permits one to separate and to obtain an accurate estimation of timing jitter contributions appearing in an analog-to-digital (A/D) converter dynamic common test setup. The results are obtained using coherent sampling configuration and are independent of quantization and nonlinearities of the converter.**

***Index Terms*—Analog-to-digital conversion, coherent sampling, curve fitting, noise measurement, timing jitter.**

I. Introduction

IMPROVEMENTS in both speed and accuracy of today's analog-to-digital (A/D) converters have significantly contributed to the increasing interest in timing jitter as a limiting factor in sampling systems [1]. An example of such a limitation is demonstrated by considering that for an ideal sampling system, with an input frequency of 10 MHz, the signal-to-noise ratio (SNR) degrades from an ideal infinite value to the theoretical SNR value of a 12-bit A/D converter with a timing jitter of 3 ps (rms). Basically, timing jitter contributions that appear in dynamic test setups for A/D converters may be classified into two main categories [1]: 1) contributions related to the test setup and 2) ontributions internally generated by the converter. As far as characterization is concerned, an accurate estimation of the two preceding quantities is a key to ensuring a robust evaluation of the device under test (DUT). An estimation of the jitter associated with the test setup should be considered to prevent an excessive bias in the measurements, as its induced defaults are implicitly set to the account of the DUT by classical characterization procedures. On the other hand, jitter internally generated by the A/D converter should be accurately estimated in order to be an intrinsic limiting factor in the product specifications.

As mentioned above, there are two main difficulties that must be solved: 1) the separation and 2) the estimation of the jitter contributions. In the work done so far, separation can be realized using two different approaches. The first approach looks at a single A/D converter with a varying input signal frequency [1]; this assumes that the A/D converter jitter is independent of the input frequency, a difficult to prove but reasonable assumption [2]. The second approach involves examining the correlation between three A/D converters driven by the same clock and signal [3]; this method is difficult to implement because a carefully designed test board is required. To contrast the few methods available for separation, there are several proposed approaches for the estimation of timing jitter contributions. A recent statistical method [2] led to accurate results by removing the limitations introduced by quantization noise and A/D converter nonlinearity which strongly influence the methods using SNR floor ratio measurement [4] or classical locked-histogram setup [5]. Although the new statistical method has demonstrated its good performance, this approach cannot be adapted to the measurement of timing jitter contributions in a dynamic test setup for A/D converters as the method uses of a slightly varying dc voltage which is not compatible with common dynamic test methods [6]. Another method was proposed in [7] and led to accurate results; the jitter is evaluated by FFT analysis but high input signal frequencies are required in order to overcome noise influence.

The purpose of this paper is to provide a new method which allows the measurement of both A/D converter internal and test setup timing jitter contributions while keeping compatibility with the dynamic characterization procedures. The theoretical aspects of this new method are presented in Section II. In Section III, the validity and the robustness of the new method are verified with experimental results.

II. Theoretical Model and Simulation Results

In sinewave testing of A/D converters, a sinusoid is uniformly sampled N_0 times with a sampling frequency f_s whose value is determined by $f_s = (N_0/K_0)f_0$, where (N_0, K_0) are relatively prime numbers and f_0 represents the input signal frequency [6]. Using a double-channel acquisition system[1] represented in Fig. 1, the nominal sampled data streams $\{v_i(n)\}$ $(i = 1, 2)$ associated with the two channels are given by

$$v_i(n) = V_i \cos\left[2\pi \frac{nK_0}{N_0} + \phi_i\right] + q_i(n) \quad \forall\, n \in \mathbb{I}_{N_0} \tag{1}$$

where

- V_i and ϕ_i amplitude and phase of the input signals, respectively;
- $q_i(n)$ quantization noise;
- $\mathbb{I}_{N_0}$ $= \{0, \cdots, N_0-1\}$.

When both timing jitter and noise are taken into account the sampled data streams $\{v_i(n)\}$ can be rewritten as [8]

$$\begin{aligned} v_i(n) = V_i \cos\left[2\pi \frac{nK_0}{N_0} + \phi_i + J_i(n)\right] \\ + b_i(n) + q_i(n) \quad \forall\, n \in \mathbb{I}_{N_0} \end{aligned} \tag{2}$$

[1]Which is based on the use of two converters driven by the same clock and input signals with shifted phases.

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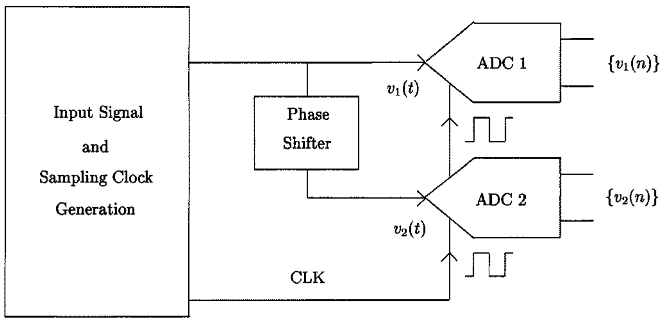

Fig. 1. Double-channel acquisition system.

where $b_i(n)$ accounts for additive thermal noise and $J_i(n)$ represents a phase uncertainty term which may be expressed with respect to the several timing uncertainties as

$$J_i(n) = (2\pi f_0)[\delta t_{jTS}(n) + \delta t_{jAD(i)}(n)] \tag{3}$$

where the random variable $\delta t_{jTS}(n)$ represents the jitter contribution associated with the test setup, while $\delta t_{jAD(i)}(n)$ is related to the internal jitter of the A/D converter. To ensure an entirely random behavior of the internal jitter we consider that the contribution is essentially generated by the clock buffer of the A/D converter [9]. The orders of magnitude which are usually encountered for jitter contributions in dynamic test setups allow the assumption $|J_i(n)| \ll 1$, thus a first order Taylor series expansion easily shows that (2) can be approximated as

$$v_i(n) = V_i \cos[\theta_i(n)] + \epsilon_i(n) \quad \forall\, n \in \mathbb{I}_{N_0} \tag{4}$$

where $\theta_i(n)$ represents the nominal sampling phase whose expression is given by

$$\theta_i(n) = 2\pi \frac{nK_0}{N_0} + \phi_i \tag{5}$$

while $\epsilon_i(n)$ represents the global noise associated with the single-channel i and defined by

$$\epsilon_i(n) = -\psi_i(n) J_i(n) + b_i(n) + q_i(n) \quad \forall\, n \in \mathbb{I}_{N_0} \tag{6}$$

with

$$\psi_i(n) = V_i \sin[\theta_i(n)] \quad \forall\, n \in \mathbb{I}_{N_0}. \tag{7}$$

In order to get insight the statistical properties of the output noises associated with the two channels, the random variables $\delta t_{jTS}(n)$, $\delta t_{jAD(1)}(n)$ and $\delta t_{jAD(2)}(n)$ are assumed to be independent[2] with zero means and variances, respectively, given by σ^2_{jTS}, $\sigma^2_{jAD(1)}$ and $\sigma^2_{jAD(2)}$. As a consequence the two phase uncertainty terms $J_i(n)$ also represent some random variables with zero mean and variances given by

$$\sigma^2_{J_i} = \sigma_0^2 + \sigma_i^2 \tag{8}$$

with

$$\begin{aligned} \sigma_0^2 &= (2\pi f_0)^2 \sigma^2_{jTS} \\ \sigma_i^2 &= (2\pi f_0)^2 \sigma^2_{jAD(i)}. \end{aligned}$$

[2]This assumption is justified as the jitter contributions associated with the A/D converters are internally generated.

Under these assumptions, the variances of the output noises, $\epsilon_i(n)$, are expressed by

$$\sigma^2[\epsilon_i(n)] = \sigma^2_{J_i} \psi_i^2(n) + \sigma^2_{b_i} + \frac{q^2}{12} \quad \forall\, n \in \mathbb{I}_{N_0}. \tag{9}$$

Equation (9) represents an extension to the dynamic case, already found in [7], of the well-known expression of the variance associated with the timing uncertainties plus noise obtained for the locked histogram configuration [2]. Assuming that the statistical properties of the timing uncertainties are time invariant,[3] an experimental evaluation of (9) can be obtained by acquiring $N_0 \times M_0$ contiguous samples for each channel where M_0 is assumed to be an even number. The samples are now indexed by $n + mN_0$, where two parameters (n, m) describe, respectively, the two sets $\mathbb{I}_{N_0} = \{0, \cdots, N_0 - 1\}$ and $\mathbb{I}_{M_0} = \{0, \cdots, M_0 - 1\}$. Thanks to this indexation, we obtain the relation for the nominal sampling phase

$$\theta_i(n, m) = 2\pi \frac{(n + mN_0)K_0}{N_0} + \phi_i \equiv \theta_i(n). \tag{10}$$

For an acquisition of $N_0 \times M_0$ contiguous samples, (4) has to be modified in order to use the (n, m) indexation. Using the N_0 periodicity of the sampling phase expressed by (10), the sampled data streams are given by

$$\begin{aligned} v_i(n, m) = V_i \cos[\theta_i(n)] + \epsilon_i(n, m) \\ \forall\, (n, m) \in \mathbb{I}_{N_0} \times \mathbb{I}_{M_0}. \end{aligned} \tag{11}$$

From (11), it appears that M_0 samples are obtained for each of the N_0 sampling phases $\theta_i(n)$, as shown in Fig. 2. To extract the noise contributions ϵ_i among the sampled data, we define for a given couple $(m_1, m_2) \in \mathbb{I}_{M_0} \times \mathbb{I}_{M_0}$ with $m_1 \neq m_2$

$$\begin{aligned} \Delta_i^{(m_1, m_2)}(n) &= v_i(n, m_1) - v_i(n, m_2) \\ &= \epsilon_i(n, m_1) - \epsilon_i(n, m_2). \end{aligned} \tag{12}$$

Using common mean and variance statistical estimators applied to one sequence composed of $M_0/2$ independent $\Delta_i^{(m_1, m_2)}(n)$ it can be shown that the following quantities:

$$\sigma^2[\Delta_i(n)] = \frac{2}{M_0} \sum [\Delta_i^{(m_1, m_2)}(n) - \overline{\Delta_i}(n)]^2 \tag{13}$$

with

$$\overline{\Delta_i}(n) = \frac{2}{M_0} \sum \Delta_i^{(m_1, m_2)}(n) \tag{14}$$

satisfy

$$\begin{aligned} &\lim_{M_0 \to +\infty} [\sigma^2[\Delta_i(n)]] \\ &\quad = 2[\sigma_0^2 + \sigma_i^2]\psi_i^2(n) + 2\sigma^2_{b_i} + \frac{q^2}{6}, \quad \forall\, n \in \mathbb{I}_{N_0}. \end{aligned} \tag{15}$$

To make use of the correlation which exists between the two channels of the acquisition system, it is useful to define

$$\Delta_3^{(m_1, m_2)}(n) = \Delta_2^{(m_1, m_2)}(n) - \Delta_1^{(m_1, m_2)}(n) \tag{16}$$

[3]As mentioned in [8] this assumption might not be accurate in some special cases.

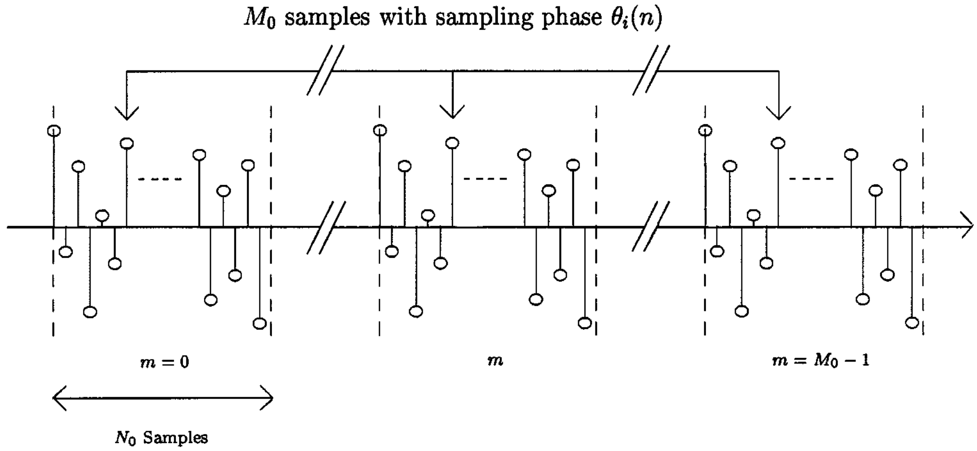

Fig. 2. Graphical representation of the $N_0 \times M_0$ contiguous samples.

from which it can be derived

$$\lim_{M_0 \to +\infty} [\sigma^2[\Delta_3(n)]] = 2 \sum_{h=0}^{2} \sigma_h^2 \psi_h^2(n) + 2[\sigma_{b_1}^2 + \sigma_{b_2}^2] + \frac{q^2}{3}, \quad \forall\, n \in \mathbb{I}_{N_0}. \tag{17}$$

with

$$\psi_0^2(n) = (V_1 \;\sin[\theta_1(n)] - V_2 \sin[\theta_2(n)])^2 \quad \forall\, n \in \mathbb{I}_{N_0}. \tag{18}$$

Hence, (15) and (17) define three sets of N_0 equations from which it is possible to estimate the set of unknowns $\{\sigma_0, \sigma_1, \sigma_2, \sigma_{b_1}, \sigma_{b_2}\}$ using least-squares (LS). First of all, the thermal plus quantization noise contributions are estimated using the two models defined by (15), then to avoid matrix singularities these two quantities are combined with (17) which can be formally rewritten assuming that M_0 is sufficiently large

$$\widetilde{\sigma^2}[\Delta_3(n)] \simeq 2[\sigma_0^2 \psi_0^2(n) + \sigma_1^2 \psi_1^2(n) + \sigma_2^2 \psi_2^2(n)] \tag{19}$$

with

$$\widetilde{\sigma^2}[\Delta_3(n)] = \sigma^2[\Delta_3(n)] - 2\left[\widehat{\sigma_{b_1}^2} + \widehat{\sigma_{b_2}^2} + \frac{q^2}{6}\right] \quad \forall\, n \in \mathbb{I}_{N_0}. \tag{20}$$

As a consequence, the design matrix $\mathbf{A}$ used for the estimation of the timing uncertainty contributions is a $(N_0, 3)$ matrix given by

$$\mathbf{A} = 2 \begin{pmatrix} \psi_0^2(0) & \psi_1^2(0) & \psi_2^2(0) \\ \vdots & \vdots & \vdots \\ \psi_0^2(n) & \psi_1^2(n) & \psi_2^2(n) \\ \vdots & \vdots & \vdots \\ \psi_0^2(N_0-1) & \psi_1^2(N_0-1) & \psi_2^2(N_0-1) \end{pmatrix}. \tag{21}$$

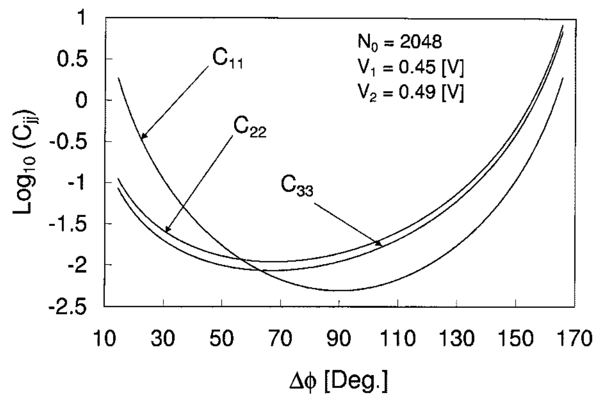

Fig. 3. Minimization of coefficient C_{11} by use of the phase difference $\Delta\phi$

In order to minimize the standard deviation of the estimated parameter σ_{jTS} as this contribution is usually the dominant one, the term C_{11} of the matrix $\mathbf{C}$ defined by

$$\mathbf{C} = (\mathbf{A}^T \mathbf{A})^{-1} \tag{22}$$

where $\mathbf{A}^T$ represents the transpose of the matrix $\mathbf{A}$, has to be minimized [10]. This minimization is achieved by setting

$$\Delta\phi = \theta_1(n) - \theta_2(n) = \phi_1 - \phi_2 \tag{23}$$

to an optimal value given by $\Delta\phi = \pi/2$, as shown in Fig. 3. As the measurement errors are not normally distributed, the quantitative information on the standard deviation of the estimated parameters cannot be obtained by classical formulas associated with LS methods [10]. Thus to evaluate the error estimations on the parameters, and to use all the statistical information available, it can be noticed that Ω_{M0} sets composed of $M_0/2$ independent elements $\Delta_i^{(m_1,m_2)}(n)$ can be extracted from $\{v_i(n,m)\}$ by use of (12) where Ω_{M0} is given by a product of binomial coefficients whose value is

$$\Omega_{M0} = \prod_{i=0}^{M_0/2-1} \binom{M_0 - 2i}{2} = (M_0)!2^{-(M_0/2)}. \tag{24}$$

The use of these so-called extracted sets[4] then allows one to achieve several parameter estimations from which it is possible to obtain an evaluation of the means and standard deviations of the root mean square values associated with the estimated timing uncertainties and noise contributions (bootstrap method [10]). To validate the algorithm the method was applied to a simulated ideal 12-bit A/D converter using the conditions given in Table I and assuming Gaussian distributions of timing jitters and thermal noises. The simulated and estimated root mean square values are given in Table II where 50 randomly choosen sets have been used for the estimations of standard deviations associated with the estimated parameters. As far as the simulation is concerned the method led to accurate results, both in estimated values and associated confidence limits. The model (17) seems acceptable to fit the data as shown in Fig. 4, where an example of a standard deviation, $\sigma[\Delta_3(n)]$, and its LS fitted curve obtained from a single extracted set composed of $M_0/2$ independent $\Delta_i^{(m_1,m_2)}(n)$ are given.[5] The statistical behavior of the method was verified by calculating the standard deviation, $\sigma_{\sigma jTS}$, of the estimated root mean square value of the test setup jitter as a function of the number of samples N_0.

For such an estimation the relation between $\sigma_{\sigma jTS}$ and N_0 should be ideally given by

$$\log(\sigma_{\sigma jTS}) = -\tfrac{1}{2}\log(N_0) + C \tag{25}$$

where C represents a constant with respect to the parameter N_0 and the actual σ_{jTS}. As shown in Fig. 5, the slope of the regression line associated with the simulated data is equal to -0.47. This value seems sufficiently close to the theoretical value of -0.5 to ensure a good statistical behavior of the algorithm.

TABLE I
PARAMETERS USED FOR THE SIMULATION

N_0	M_0	f_0	f_s	$\Delta\phi$
2048	128	20 MHz	50 MHz	92.8 Deg.

TABLE II
SIMULATED AND ESTIMATED TIMING UNCERTAINTIES AND NOISES

	Simulated	Estimated	Std. Dev.
σ_{jTS}	2.5 ps	2.494 ps	15.66 fs
$\sigma_{jAD(1)}$	1 ps	0.970 ps	78.64 fs
$\sigma_{jAD(2)}$	0.75 ps	0.811 ps	65.34 fs
σ_{b_1}	0.55 LSB	0.542 LSB	2.49 10^{-3} LSB
σ_{b_2}	0.5 LSB	0.492 LSB	1.97 10^{-3} LSB

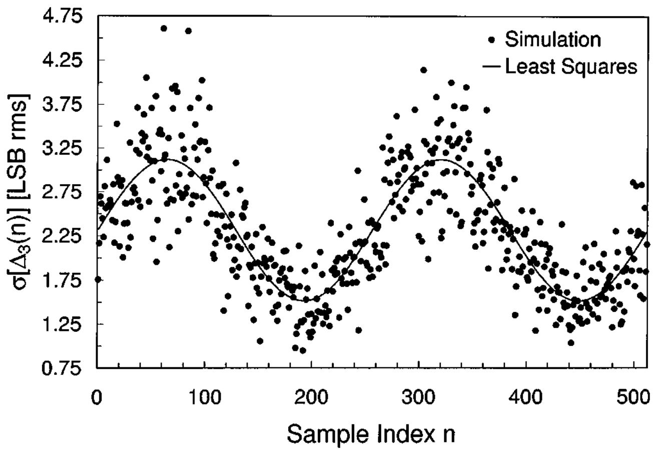

Fig. 4. Example of the $\sigma[\Delta_3(n)]$ curve and its associated LS fit for $N_0 = 512$.

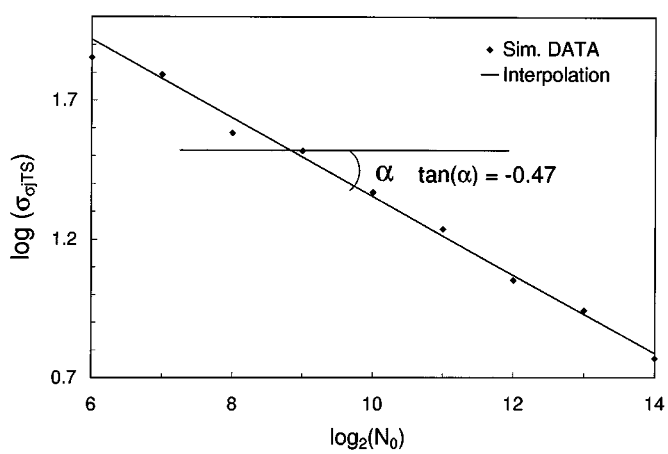

Fig. 5. Standard deviation of the estimated test setup jitter.

III. EXPERIMENTAL RESULTS

The method was applied to the timing jitter contributions measurement of a 12-bit 70 MSPS A/D converter (Philips TDA8768A) test setup given in Fig. 6. The generation of input and clock signals is based on the use of two synthesizers with low phase noise synchronized by a single ultra stable oscillator in order to minimize the intrinsic jitter of the test setup. A sinewave $v(t)$ of frequency f_0 feeds a quadrature hybrid splitter whose outputs $v_1(t)$ and $v_2(t)$ are input signals of the two A/D converters. The phase shift of these two sinewaves is specified to be in the range 90°±3° for input frequencies in the band 20–140 MHz. These specifications meet the requirements of the method as the variations of C_{11} in a vicinity of $\Delta\phi = 90°$ are sufficiently small (see Fig. 3) to avoid excessive degradation of the algorithm results. Because a square wave is required as a clock signal, the sinewave $s(t)$ of frequency f_s and amplitude V_s delivered by the synthesizer is used as an external trigger source to a low jitter pulse generator. Some noise generated by an arbitrary waveform generator (AWG) is added to the external trigger source $s(t)$ in order to vary the standard deviation of the jitter associated with the test setup. Due to an ac-coupling input the input frequencies of $s(t)$ are specified to be in the range 33 MHz–3 GHz. Hence, the frequency band of the noise generated by the AWG was set to 50–150 MHz in order to minimize the filtering effects which may occur in the input stage of the pulse generator. Several estimations of the jitter contributions were made as a function of the rms value

[4]As an example, for $M_0 = 4$ the following extracted sets are obtained

$$\begin{array}{ll}\{\Delta_i^{(1,2)}(n), \Delta_i^{(3,4)}(n)\} & \{\Delta_i^{(1,3)}(n), \Delta_i^{(2,4)}(n)\} \\ \{\Delta_i^{(1,4)}(n), \Delta_i^{(2,3)}(n)\} & \{\Delta_i^{(3,4)}(n), \Delta_i^{(1,2)}(n)\} \\ \{\Delta_i^{(2,4)}(n), \Delta_i^{(1,3)}(n)\} & \{\Delta_i^{(2,3)}(n), \Delta_i^{(1,4)}(n)\}\end{array}$$

[5]Note that for convenience the curves have been reconstructed by use of a sort algorithm which performs a sampling rate conversion up to $f_s = N_0 f_0$.

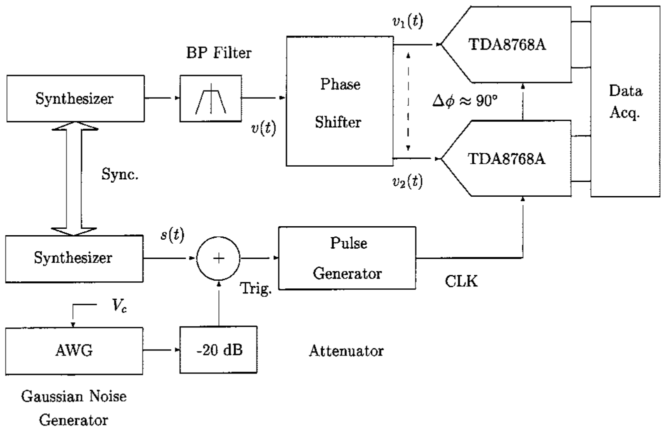

Fig. 6. Block diagram of the experimental setup.

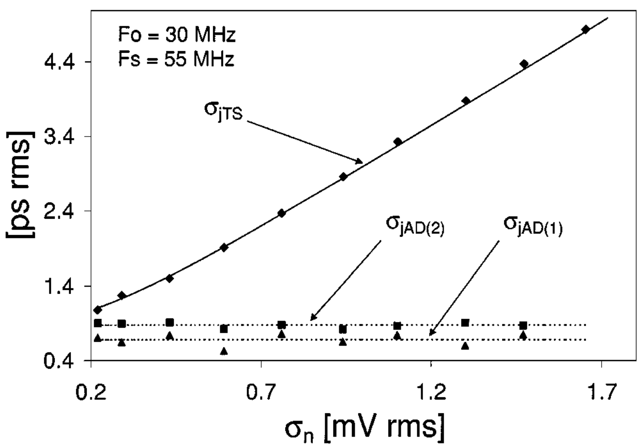

Fig. 7. Test setup and A/D converter jitter measures as a function of σ_n.

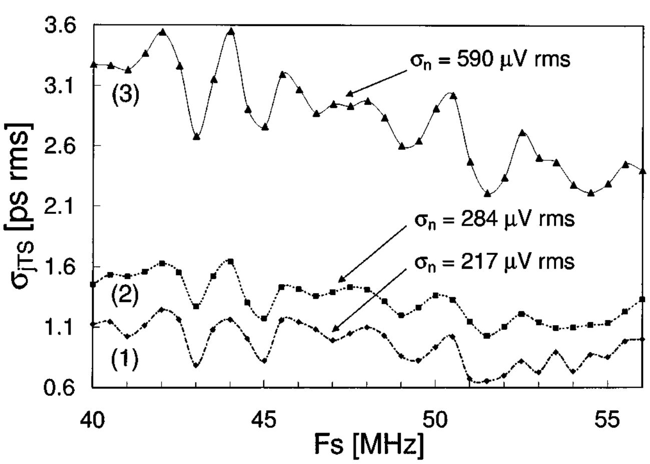

Fig. 8. Test setup jitter as a function of sample frequency and noise.

σ_n of the noise generated by the AWG.[6] Using $N_0 = 4096$ and $M_0 = 32$, results are shown in Fig. 7 for the frequency configuration $f_0 = 30$ MHz and $f_s \approx 55$ MHz.[7] The measures, $\sigma_{jAD(i)}$, of the converters were found to be independent of σ_n

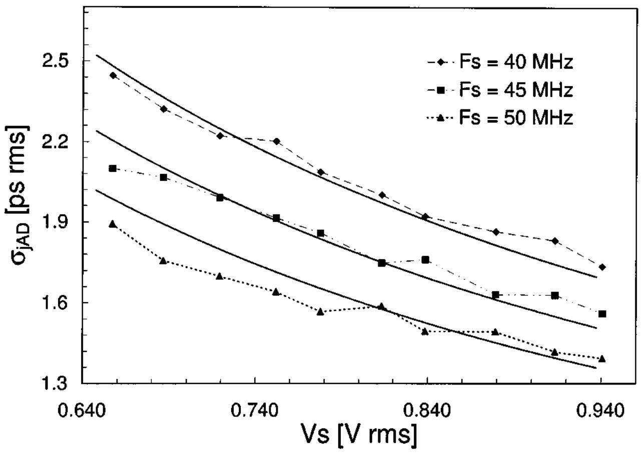

Fig. 9. A/D converter jitter measures as a function of V_s and sample frequency.

with mean values of 683 fs and 881 fs. The jitter associated with the test setup, σ_{jTS}, may be experimentaly expressed by

$$\sigma_{jTS}^2 = K(f_s) \cdot \sigma_n^2 + \sigma_{jTS(0)}^2(f_s) \tag{26}$$

where $K(f_s)$ represents a conversion factor and $\sigma_{jTS(0)}(f_s)$ is a jitter contribution which is independent of σ_n. For the test setup which was used, it can be shown that the conversion factor $K(f_s)$ cannot be expressed by the relation given in [9], i.e.

$$K(f_s) \neq \frac{1}{(\pi V_s f_s)^2}. \tag{27}$$

In fact, several estimations of σ_{jTS} as a function of f_s have been made for different values of σ_n and are given in Fig. 8. The correlations between the three curves were found to be given by $\mathrm{corr}[1,2] = 0.89$, $\mathrm{corr}[1,3] = 0.84$, and $\mathrm{corr}[2,3] = 0.94$ which clearly indicates a deterministic behavior different from the one given in [9] of the conversion factor with respect to f_s. This result can be reasonably accepted considering that the equivalent model of the input stage of the pulse generator is much more complicated than the one which is used in [9]. One the other hand, when the sinewave, $s(t)$, is directly used as the clock signal of the two converters without added noise, the behavior of the aperture uncertainty is well described by

$$\sigma_{jAD} = \frac{\sigma_{\mathrm{in}}}{\pi V_s f_s} \tag{28}$$

where σ_{in} represents the equivalent input noise of the converter. As shown in Fig. 9, where a jitter contribution σ_{jAD} has been measured as a function of V_s for different sample frequencies and $f_0 = 30$ MHz. Due to (28), an evaluated value of $\sigma_{\mathrm{in}} = 195\ \mu$V rms gives rise to an acceptable description of the data. The estimated value of σ_{in} agrees with simulation results which were obtained for the converter, consequently, a validation of the estimated jitter contribution is obtained.

IV. Conclusions

The method presented in this paper provides an accurate measurement of timing jitter contributions which are encountered in a dynamic test setup for an A/D converter. Unlike other existing

[6]The rms values σ_n as a function of the control voltage, V_c, were evaluated using histogram measurements.

[7]The actual coherent sampling frequency is $f_s = (4096/2235)f_0 = 54.979\,865$ MHz.

methods, it uses two A/D converter paths and allows the separation and the measurement of test setup jitter and internal jitter of A/D converter. Simulation and experimental results confirm that the method is able to give accurate results.

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REFERENCES

[1] M. Shinagawa, Y. Akazawa, and T. Wakimoto, "Jitter analysis of high-speed sampling systems," *IEEE J. Solid-State Circuits*, vol. 25, pp. 220–224, Feb. 1990.

[2] G. Chiorboli, M. Fontanili, and C. Morandi, "A new method for estimating the aperture uncertainty of A/D converters," *IEEE Trans. Instrum. Meas.*, vol. 47, pp. 61–64, Feb. 1998.

[3] Y. Langard, J. L. Balat, and J. Durand, "An improved method of ADC jitter measurement," in *Proc. ITC*, 1994, pp. 763–770.

[4] Y. C. Jenq, "Digital spectra of nonumiformly sampled signals: Theories and applications—Measuring clock/aperture jitter of an A/D system," *IEEE Trans. Instrum. Meas.*, vol. 39, pp. 969–971, Dec. 1990.

[5] Dynamic performances testing of A to D converters, in *Hewlett Packard Product Note 5180A-2*, Hewlett Packard Company, 1982.

[6] *IEEE Draft Standard for Terminology and Test Methods for Analog-to-Digital Converters*, IEEE Std. 1241, 1996.

[7] D. M. Hummels, W. Ahmed, and F. H. Irons, "Measurement of random sample time jitter for ADCs," in *Proc. IEEE Int Symp. Circuits Syst.*, Seattle, WA, May 1995, pp. 708–711.

[8] S. S. A. Awad, "The effects of accumulated timing jitter on some sinewave measurements," *IEEE Trans. Instrum. Meas.*, vol. 44, pp. 945–951, Oct. 1995.

[9] R. van de Plassche, *Integrated Analog-to-Digital and Digital-to-Analog Converters*. Norwell, MA: Kluwer, 1994.

[10] W. H. Press, S. A. Teukolsky, W. T. Vetterling, and B. P. Flannery, *Numerical Recipes in C*. Cambridge, U.K.: Cambridge Univ. Press, 1992.

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